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Pioneer-Central

FREQUENCY TEMPERATURE COMPENSATION TECHNIQUES FOR QUARTZ CRYSTAL OSCILLATORS

FIRST QUARTERLY REPORT

PIONEER-CENTRAL DIVISION
DAVENPORT, IOWA

THE Bendix CORPORATION

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RESEARCH WORK FOR

FREQUENCY TEMPERATURE COMPENSATION

TECHNIQUES FOR QUARTZ CRYSTAL OSCILLATORS

in conjunction with Signal Corps

Technical Requirements SCL-6610

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REPORT NO. 1

Object of Research: The design and development of circuit techniques for oven-less crystal oscillators having frequency temperature stabilities previously achieved in temperature stabilized oscillators consuming several watts of power

Prepared for
U. S. Army Signal Research
and
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Fort Monmouth, New Jersey

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1.1 Purpose

The purpose of this project is to evolve a practical analytical and empirical approach to the temperature compensation of quartz crystal oscillators. The study will encompass numerous methods of compensation, of which the most promising will be investigated fully and complete design procedure obtained. The study will be concentrated on a nominal frequency of three megacycle, but will be generally applicable to AT cut quartz crystals of from 1 to 20 megacycles.

2.1 Abstract

The mathematical analysis of five different methods of temperature compensating crystal oscillators is presented. The five methods presented are referred to as Methods A, B, B', D and E. Method A utilizes a back-biased diode and thermistors as the compensation elements. Methods B and B' utilize the junction capacitance of the transistor and thermistors in the transistor bias network for compensation. Method D uses the injector to collector junction capacitance of a binistor and a thermistor control network as the compensation elements. System E uses a forward biased diode, capacitor and thermistor control network as the compensation elements.

The results of experimental tests on the compensation circuits and/or compensated oscillator is presented. A compensation on one three-megacycle oscillator was within $\pm$ .7 parts in 10^7, from 0°C to +60°C.

3.1 Conferences

Mr. Shodowski and Mr. Layden on August 20, 1962, at The Bendix Corporation, Pioneer-Central Division

This conference covered the general organization of the project, the time schedule and the emphasis of study. The proposed time schedule was reviewed and approved. Elimination of proposed methods of compensation that do not appear feasible is to be done before the end of the 2nd Quarter. It was agreed that the investigation not be limited to the specific methods initially proposed, but that other methods also be investigated. The list below gives a summary of some of the methods and components discussed and accepted as satisfactory for investigation purposes.

Class A: Discrete Systems

1. Back-Biased Diode Capacitor
2. Variable Inductance
3. Temperature Sensitive Capacitor
4. Barium Titanate Dielectric Material
5. Electronically Variable Capacitance
6. Switching Methods

Class B: Integrated Systems

1. Transistor Method
2. Binistor Method

It was decided to discontinue the voltage regulator study that had been started until the scope of work warranted its continuance.

The final result of this project was defined as follows: The final report shall contain sufficient information to permit an engineer to compensate a quartz crystal oscillator to an accuracy within the scope of this investigation.

4.1 Varicap Compensation - Mathematical Analysis

In any frequency compensation method, a means is needed whereby a change in frequency of the crystal is produced that is equal and opposite in sense to the change caused by temperature. In the varicap method and other methods of compensation considered in this report, the means for producing a compensating frequency change is accomplished by changing the load reactance at the crystal terminals. Figure 1 shows the effect on frequency of changing the load capacitance of a crystal as a function of the crystal C_o/C_1 ratio.

A general form of frequency compensation can be illustrated as in Figure 2. The compensated oscillator is composed of an active element with associated circuitry, a crystal, a variable reactance and a control network. Figure 3 shows the equivalent schematic diagram of Figure 2 for a varicap compensated oscillator, where the transistor, resistors, capacitors, and inductors constitute the active element and associated circuitry. The crystal is connected to the active circuit, a varicap is the variable reactance, and the control network, Z_1, Z_2, and E, are composed of thermistors, resistors, and a voltage source.

Figure 4 is a simplified a-c equivalent circuit for the oscillator shown in Figure 3 and is the basis for the following analysis. It is assumed that the oscillator circuit at Terminals 1 and 2 in Figure 2 can be represented by a parallel capacitance, C_c, and negative resistance, $-R_o$. Also the assumption is made that R_s is negligible.

Equation (1) defines the change in frequency of a crystal due to a change in the capacitance presented at its terminals as shown in Figure 5. C_o, M, and $r = C_o/C_1$ are constants of the crystal, and C_x is the crystal load capacitance.

(1) $$\frac{\Delta f}{f} = P - M + \frac{C_o \times 10^6}{2r\,(C_o + C_x)}$$

In this analysis, the Q's are considered high enough that losses can be ignored. C_x is equivalent to $C_c C_d / C_c + C_d$, and Equation (2) defines P as a function of C_c and C_d where P is equal to $\Delta f/f$ in PPM. M can be found by setting P = 0 and

solving the resulting equation for M.

$$(2)\quad P = -M + \frac{C_oC_c \times 10^6}{2r\,(C_oC_c + C_oC_d + C_cC_d)} + \frac{C_oC_d \times 10^6}{2r\,(C_oC_c + C_oC_d + C_cC_d)}$$

Now if P is differentiated with respect to C_d, then (d P) as a function of (d C_d) will be obtained.

$$(3)\quad \frac{dP}{dC_d} = - \frac{C_oC_c^2 \times 10^6}{2r\,(C_oC_c + C_oC_d + C_cC_d)^2}$$

In a temperature compensated oscillator, C_d will be a varicap network and control network as shown in Figure 5. E, Z_1 and Z_2 provide the proper temperature sensitive voltage to the varicap for compensation. The equation for C_d is given approximately by Equation (4).

$$(4)\quad C_d = \frac{K}{\sqrt{V_o}}$$

Where K is a constant determined by the diode characteristics and V_o is the control voltage provided by the voltage divider shown in Figure 6.

When Equation (4) is differentiated with respect to V_o, Equations (5) and (6) are obtained.

$$(5)\quad \frac{dC_d}{dV_o} = -\frac{1}{2} KV_o^{-3/2}$$

$$(6)\quad dC_d = -\frac{1}{2} KV_o^{-3/2}\,(dV_o)$$

If Equation (6) is used to replace d C_d in Equation (3), then the derivative of P with respect to V_o is found as shown by Equation (7).

$$(7)\quad \frac{dP}{dV_o} = \frac{KV_o^{-3/2}\,C_oC_c^2 \times 10^6}{4r\,(C_oC_c + C_oC_d + C_cC_d)^2}$$

$$(8)\quad dV_o = \frac{4r\,(C_oC_c + C_oC_d + C_cC_d)^2}{KC_oC_c^2 \times 10^6} V_o^{3/2}\,(dP)$$

Therefore, from Equation (8), if the circuit parameters are known then the allowable voltage change for a given change in P at a specified voltage or C_d can be found. In a given compensated oscillator the percentage change in V_o can be determined to maintain a given ΔP. At this point, the allowable voltage change at any given V_o can be found. To further carry out the investigation, the error allowable in the voltage divider to maintain the same frequency accuracy will be found.

Figure 2 shows the complete circuit for the varicap and its voltage control. From this circuit, Equation (9) can be found.

$$V_o = E \frac{(Z_2)}{(Z_1+Z_2)} \tag{9}$$

Differentiating V_o in Equation (9) with respect to Z_1 and Z_2 results in Equations (10 and (11).

$$\frac{dV_o}{dZ_1} = \frac{-Z_2 E}{(Z_1+Z_2)^2} \tag{10}$$

$$\frac{dV_o}{dZ_2} = \frac{Z_1 E}{(Z_1+Z_2)^2}$$

At this point a new equation defining the voltage divider will be introduced by Equation (12).

$$\phi = \frac{E}{V_o} - 1 = \frac{Z_1}{Z_2} \tag{12}$$

By rearranging Equation (9), the equation for the ratio of Z_1/Z_2 is obtained and this ratio will be referred to as ϕ. This relationship for ϕ is sometimes easier to work with than the for V_o.

The derivative of ϕ with respect to V_o is given in Equation (13).

$$\frac{d\phi}{dV_o} = - \frac{E}{V_o^2} \tag{13}$$

(14) $dV_o = -\frac{V_o^2}{E}$ (dφ)

Equation (14) shows the change in V_o for a specified V_o and change in φ.

Now relating Equations (10), (11), and (14) back to Equation (8) the following relationships are obtained.

$$(15)\quad dZ_1 = -\frac{(Z_1+Z_2)^2}{Z_2 E}\quad\frac{(4r)\,(C_oC_c+C_oC_d+C_cC_d)^2}{K(C_oC_c^2 \times 10^6)}\,(dP)\,V_o^{3/2}$$

$$(16)\quad dZ_2 = \frac{(Z_1+Z_2)^2}{Z_1 E}\quad\frac{(4r)\,(C_oC_c+C_oC_d+C_cC_d)^2}{KC_oC_c^2 \times 10^6}\,(dP)\,V_o^{3/2}$$

$$(17)\quad d\phi = -\left(\frac{E}{V_o^2}\right)\quad\frac{(4r)\,(C_oC_c+C_oC_d+C_cC_d)^2}{KC_oC_c^2 \times 10^6}\,(dP)\,V_o^{3/2}$$

Another relationship that will be important when considering the stability of a given compensated oscillator is the change in P with a change in C_c. From Equation (2):

$$(18)\quad \frac{dP}{dC_c} = \frac{(C_oC_c+C_oC_d+C_dC_c)\;C_o \times 10^6 - C_oC_c \times 10^6\,(C_o+C_d)}{2r\,(C_oC_c+C_oC_d+C_cC_d)^2}$$

$$-\frac{C_oC_c \times 10^6\,(C_o+C_d)}{2r\,(C_oC_c+C_oC_d+C_cC_d)^2}$$

Therefore,

$$\frac{dP}{dC_c} = -\frac{C_oC_c^2 \times 10^6}{2r(C_oC_c+C_oC_d+C_cC_d)^2}$$

Rearranging Equation (18), the equation defining the change in C_c for a given change in P is obtained.

$$(19)\quad dC_c = \frac{-2r\,(C_oC_c+C_oC_d+C_cC_d)^2}{C_oC_d^2 \times 10^6}\,(dP)$$

Values will be assumed for the circuit shown in Figure 6 and by using the equation derived previously, the defining relationships for the oscillator will be determined.

Let $r = C_o/C_1 = 300$

$C_c = 100$ pf
$E = 15$ V
$C_o = 5$ pf
$dP = .01$ PPM

$K = 200 \times 10^{-12} f - V^{1/2}$
$C_d = K/V_o^{1/2}$

Let V_o	C_d	ϕ
1	200 pf	14
2	141.4 pf	6.5
4	100 pf	2.75
9	66.7 pf	.667
12	57.7 pf	.25

Assuming that a maximum change in frequency of 1 part in 10^8 is desired from any given parameter change, then the allowable changes in the parameter can be computed. The following table is the values obtained for this hypothetical oscillator.

MAXIMUM VARIATION IN CIRCUIT PARAMETERS FOR A MAXIMUM FREQUENCY CHANGE OF 0.01 PPM

V_o	$d C_d/d V_o-(10^{-12})$	$d C_c-(10^{-14})$	$d\phi$	$d V_o$-(mv)	$-d Z_1$
1	-100	-1.385	.00831	.555	$\frac{(Z_1+Z_2)^2}{Z_2}$ 3.70×10^{-5}
2	- 35.4	-1.416	.00298	.795	$\frac{(Z_1+Z_2)^2}{Z_2}$ 5.3×10^{-5}
4	- 12.5	-1.45	.0011	1.162	$\frac{(Z_1+Z_2)^2}{Z_2}$ 7.73×10^{-5}
9	- 3.71	-1.51	.00034	1.825	$\frac{(Z_1+Z_2)^2}{Z_2}$ $.21 \times 10^{-4}$
12	- 2.39	-1.56	.00023	2.22	$\frac{(Z_1+Z_2)^2}{Z_2}$ 1.48×10^{-4}

Column 1 is not related to (dP), but is the derivative of C_d with respect to V_o. Column 2 through 4 are the delta changes of the corresponding parameters with respect to dP, where (dP) = .01 PPM, as a function of V_o.

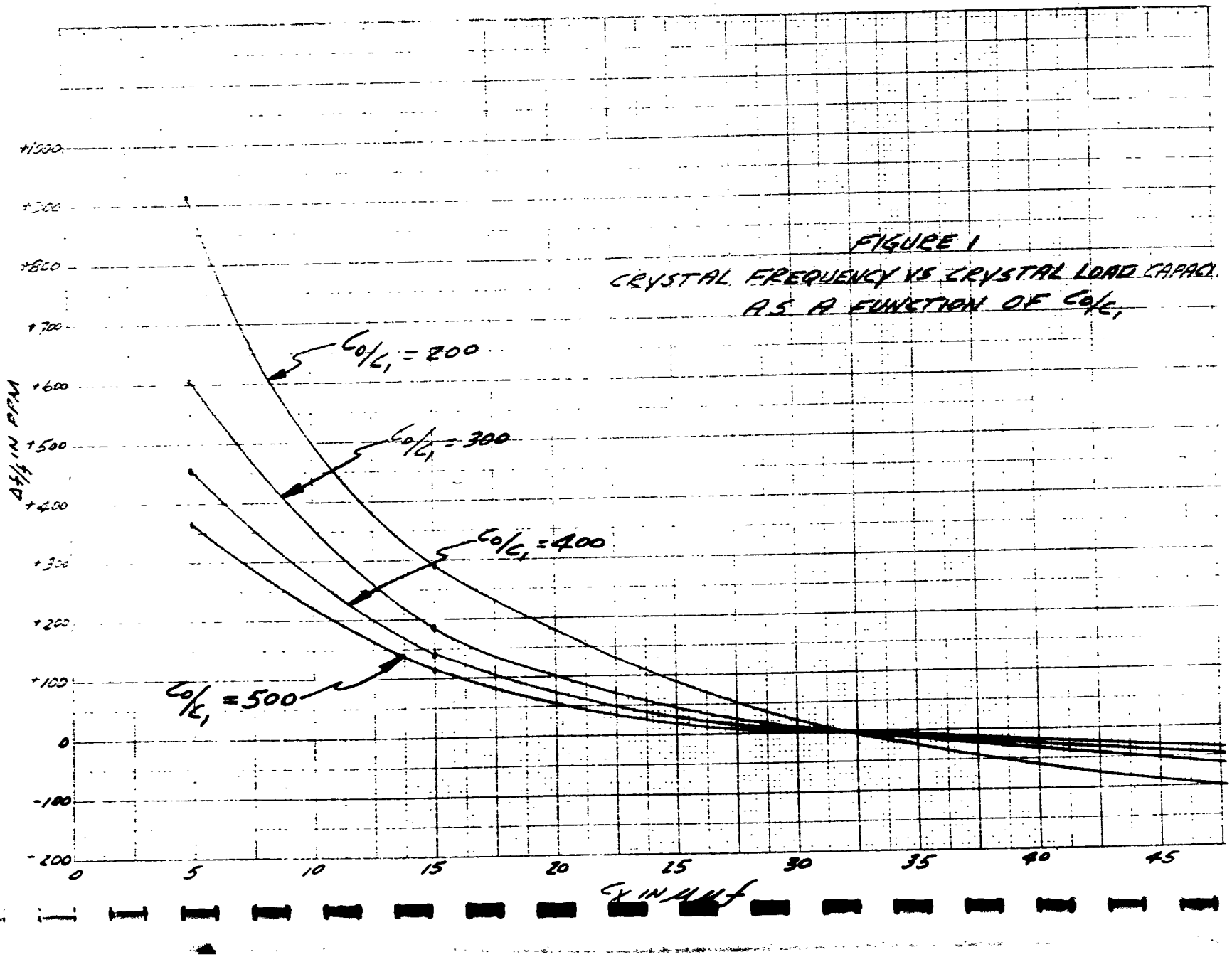
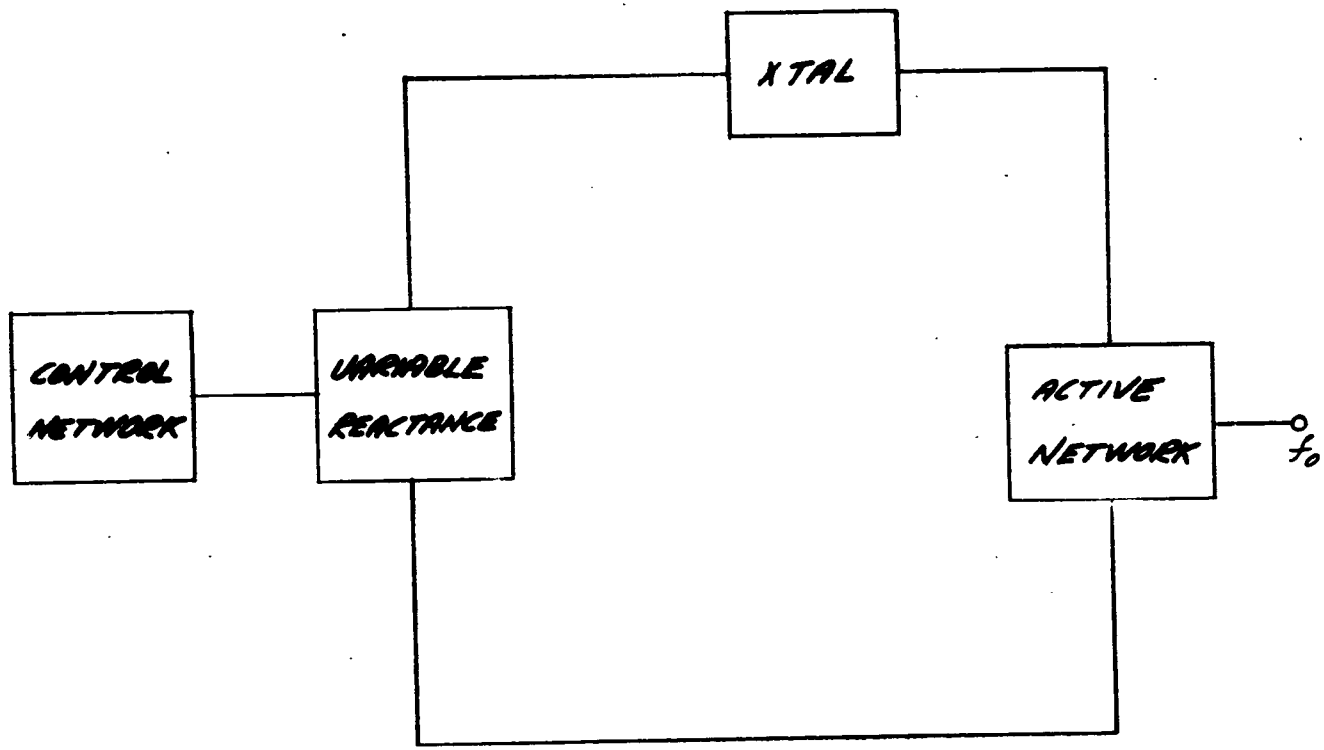
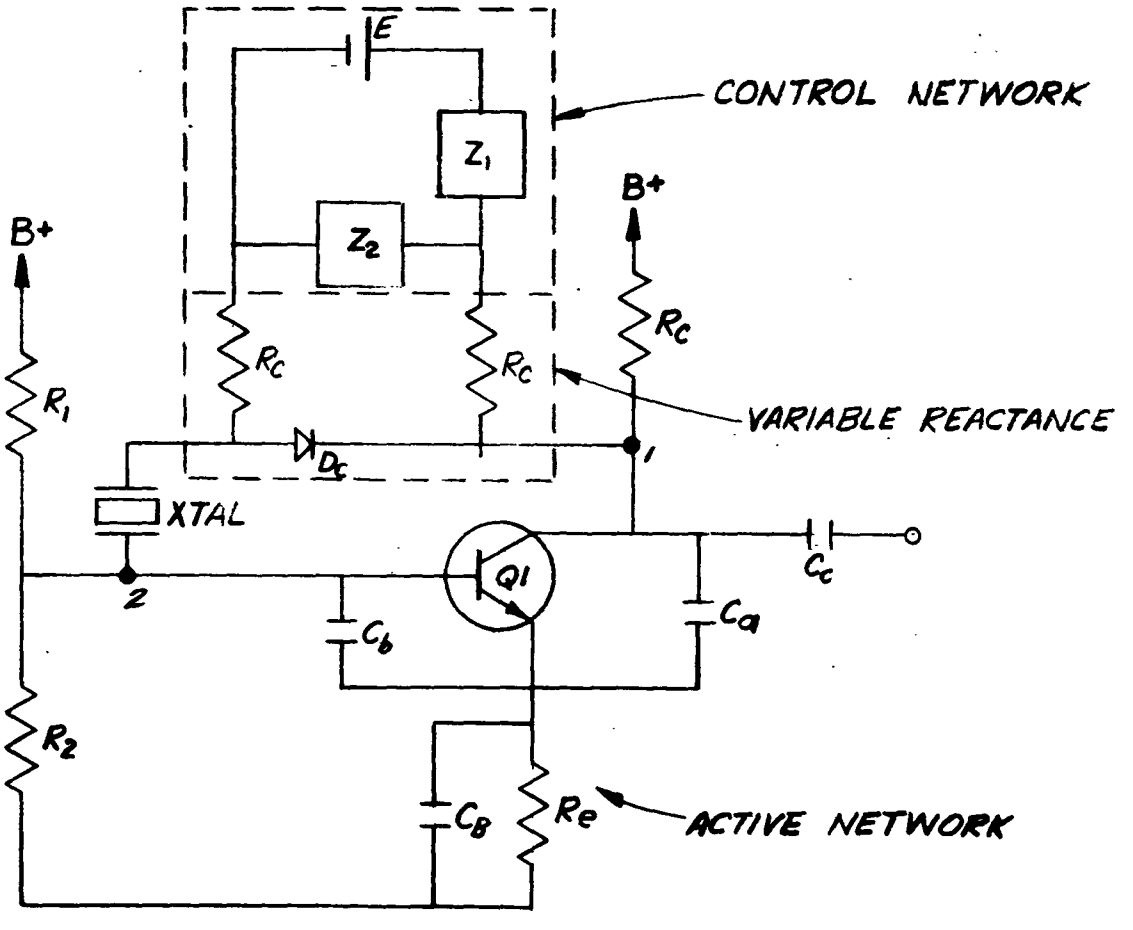


FIGURE 1
CRYSTAL FREQUENCY VS CRYSTAL LOAD CAPACI.
AS A FUNCTION OF Co/C1
Co/C1 = 200
Co/C1 = 300
Co/C1 = 400
Co/C1 = 500
Δf/f IN PPM
+1000
+900
+800
+700
+600
+500
+400
+300
+200
+100
0
-100
-200
0
5
10
15
20
25
30
35
40
45
CX IN pf



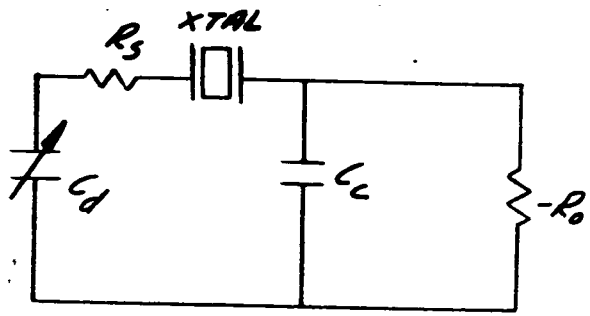
FREQUENCY COMPENSATION DIAGRAM

FIGURE 2



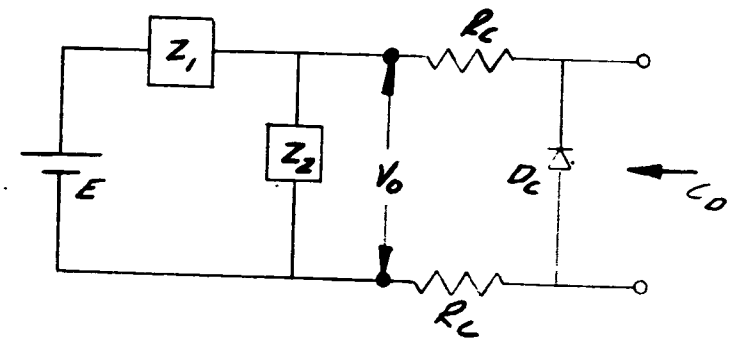
EQUIVALENT CIRCUIT FOR A VARICAP COMPENSATED OSCILLATOR

FIGURE 3



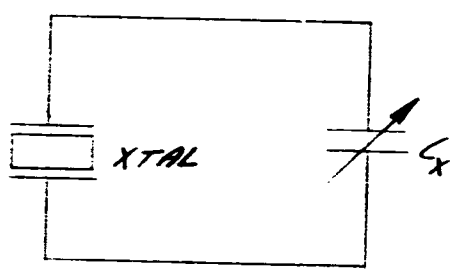
A-C EQUIVALENT CIRCUIT

FIGURE 4



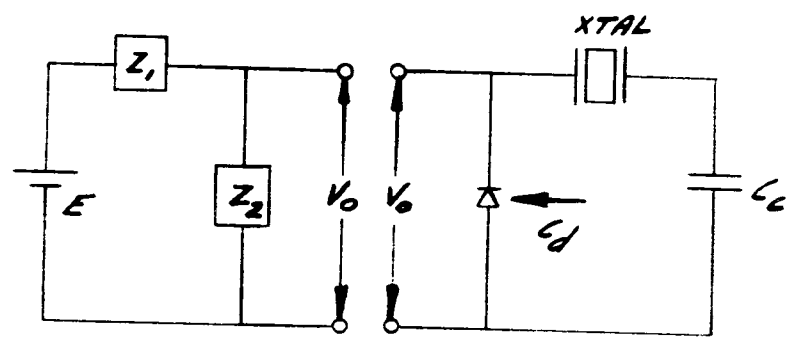
VOLTAGE DIVIDER

FIGURE 6



VARICAP NETWORK

FIGURE 5



COMPENSATION NETWORK

FIGURE 7

4.2 Varicap Compensation Empirical Data

The varicap method of compensation has also been investigated empirically. A number of oscillators using this method of compensation have been constructed and their characteristics investigated. Figure 3 is the basic oscillator configuration used in the construction of the test oscillators. Figure 6 is the basic compensation network used.

Tests were run on a number of oscillators to determine the exact characteristic exhibited by the oscillator due to changes in the circuit parameters. The first test that was made was to determine the change in frequency due to a change in supply voltage. There are two possible results from the experiment depending upon the manner in which the bias voltage, E, is obtained. If (B+) in Figure 3 is also (E), then a change in frequency due to a change in voltage will be due to two effects. One effect will be the change in capacitance of the compensation network due to a change in voltage on the varicap and the other will be the change in frequency due to changing only the B+ voltage on the oscillator.

The voltage, V_o, will not be equal to E, but will be directly proportional to E. The relationship is $V_o = (Z_2/Z_1 + Z_2)E$. Therefore, the effect of an incremental change of E on the frequency will depend upon the factor $Z_2/(Z_1+Z_2)$. Where Z_1 and Z_2 are temperature varying, the effect of Z_1 and Z_2 will have to be taken into account when determining the maximum allowable voltage deviation. A curve of $\Delta f/f$ versus B+ is shown in Figure 8, for the connection where separate power supplies are used for E and B+. If B+ was also E, the curve obtained would be the sum of the two variations discussed. The exact magnitude of resultant variations in this case would depend upon the values of B+, Z_1 and Z_2.

From the curve in Figure 8, the slope $(\Delta f/f)/\Delta V$ can be determined. At any given bias point, say V_1 in Figure 8, the maximum voltage deviation can be found for a given deviation in frequency. At V_1 in Figure 8 the value $(\Delta f/f)/\Delta V$ is equal to (N) where in this case N = .23 PPM/volt. If the assumption is made that

0.01 PPM is the maximum frequency deviation that can be tolerated due to voltage change, then the allowable voltage deviation is:

$$0.01\text{PPM} / \Delta f/f/\Delta V = 0.01 \text{ PPM/N} = 0.0435 \text{ volts}$$

The values of N can be reduced by selecting components, (transistors, capacitors, etc.) that are affected less by voltage and by selecting a different bias point (V_1).

The next experiment that was performed on these oscillators was to determine the pullability of the compensating varicap, e.i. P/V_o. Figure 9 is a set of curves of P versus V_o for different types of varicaps. If a certain voltage range for V_o is desired, the curves in Figure 9 indicate the total allowable frequency deviation that can be compensated for by using a particular varicap.

In Figure 10, the effect of changing the voltage variation of the compensation capacitance seen by the crystal and oscillator circuit is shown. These curves were obtained by putting capacitance in parallel with the varicap and increasing the series inductance until the frequency was f_o , when V_o equals five volts. The change is the characteristics of the $\Delta f/f/V$ slope is indicated in Figure 10.

The effect of changing transistors in the oscillator was not detectable and is assumed to be negligible. If a coil is used in series with the crystal for means of frequency setting, compensation characteristics may be altered over temperature of the coil due to the temperature sensitivity. Extensive tests have not been performed as yet to determine the temperature effect of the coils. Two varicaps were tried in the same circuit to determine how much the P versus V_o curve would change from one unit to another of the same type. Negligible difference was found, but a more extensive analysis of the effect of component tolerances of compensation characteristics is now in progress.

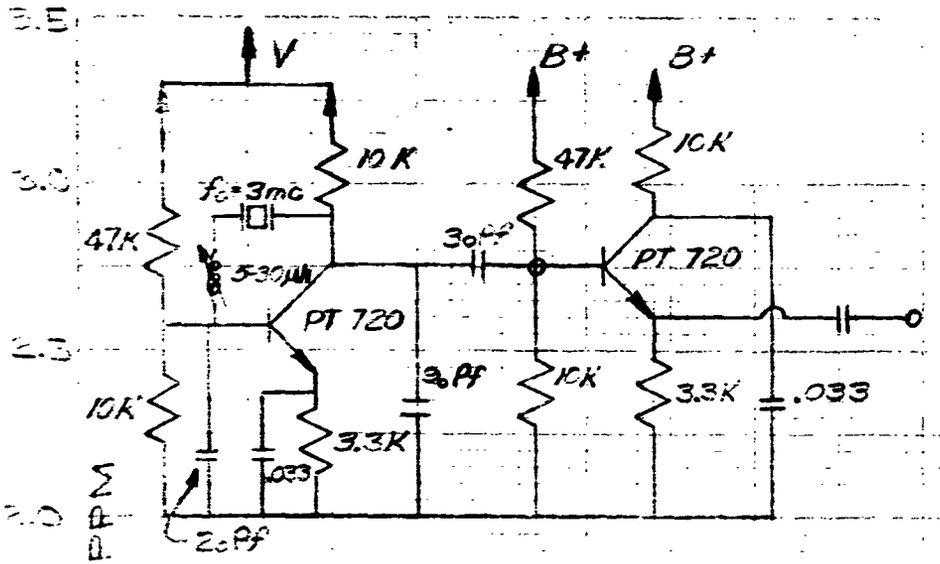
A set of curves of V_o versus temperature required to compensate crystals with the temperature coefficient shown in Figure 11 was determined from a typical curve as shown in Figure 9. This was done to get an idea of what the typical V_o versus temperature characteristics of a compensated network would have to be to compensate crystals with

various angles of cuts. Figure 12 shows the resulting V_o versus temperature curves. To generate these V_o versus temperature curves, the corresponding compensation networks required for obtaining the different curves are also shown. The difference in the basic network for different angles of cut is due to the fact that the upper and lower turning points change as the angle of cut changes; and in turn, this changes the slope of the compensation curve at various temperatures.

An oscillator was compensated using the varicap method. Two tries were all that were required to bring the oscillator total deviation to 7 PPM. The final curve of the compensated oscillator is shown in Figure 13. Thirty PPM was the $\Delta f/f$ between turning points of the uncompensated oscillator. From the experience obtained of this compensated oscillator, it appears that compensation techniques can be developed to readily compensate an oscillator with the required frequency tolerances.

FIGURE 8

FREQUENCY DEVIATION VS SUPPLY VOLTAGE



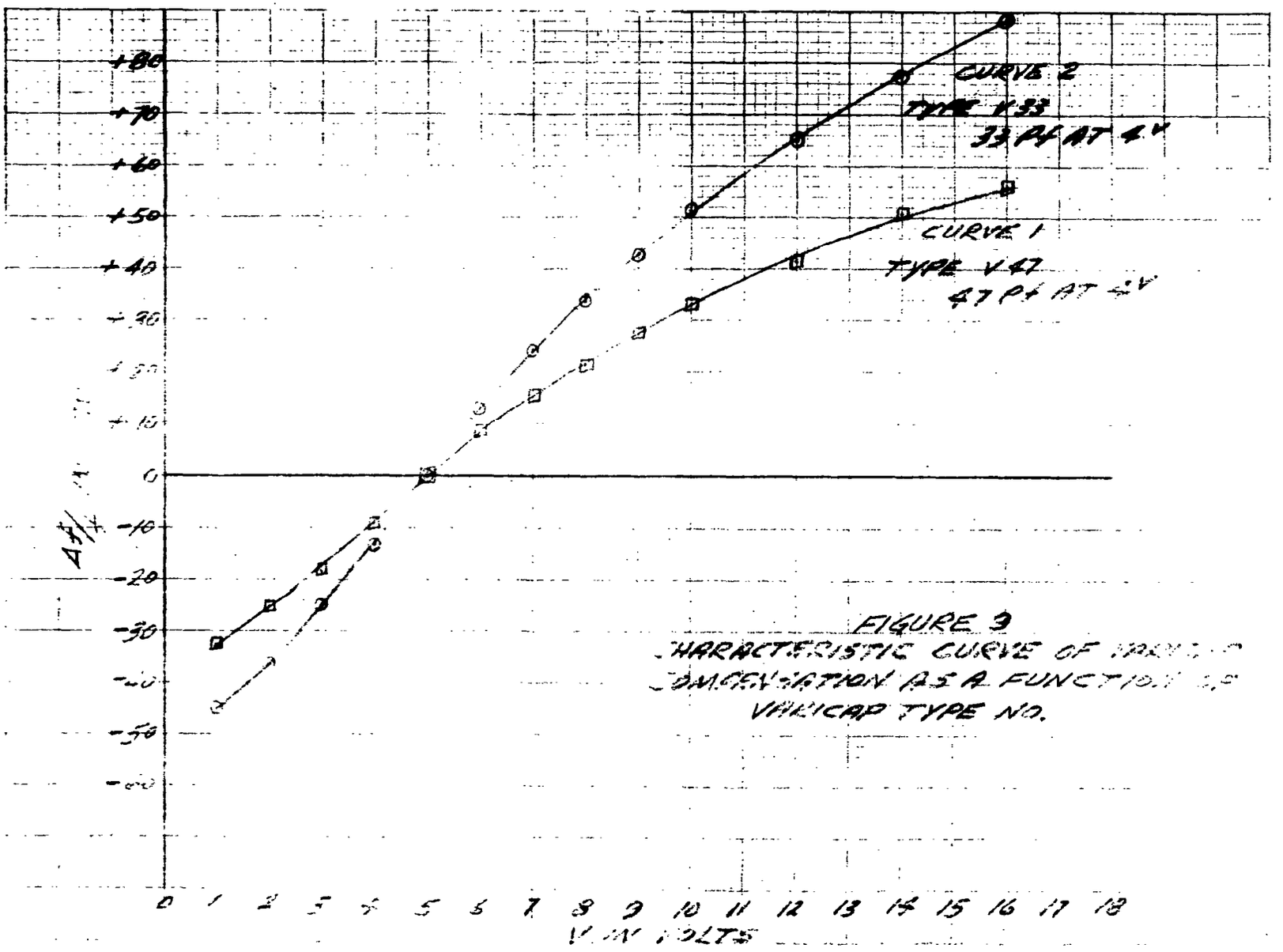


FIGURE 3
CHARACTERISTIC CURVE OF [illegible]
CAPACITANCE AS A FUNCTION OF
VARICAP TYPE NO.

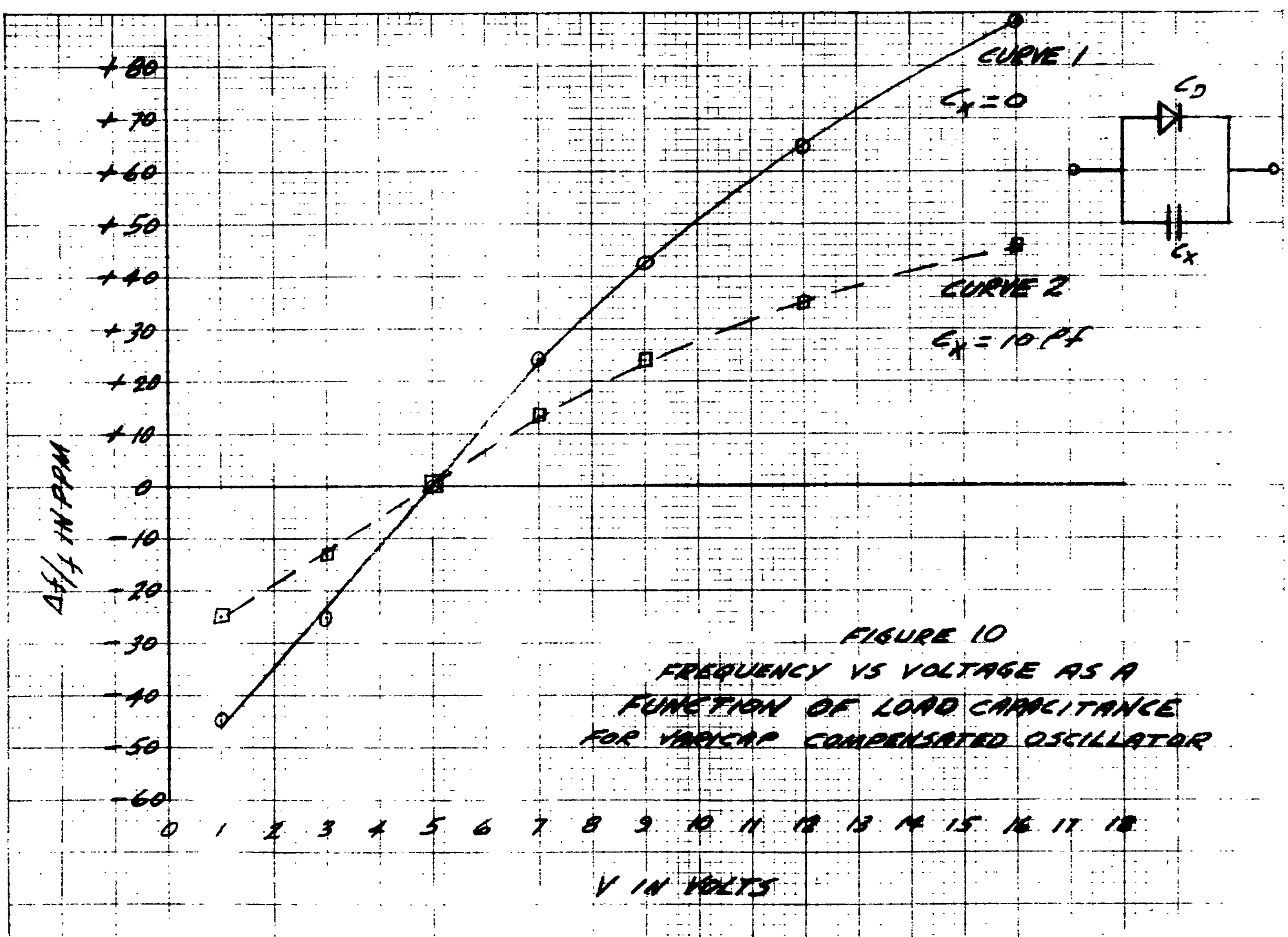


FIGURE 10
FREQUENCY VS VOLTAGE AS A FUNCTION OF LOAD CAPACITANCE FOR VARICAP COMPENSATED OSCILLATOR

FIGURE 11

FREQUENCY-TEMPERATURE CURVES-GENERALIZED FOR AT CUT CRYSTALS

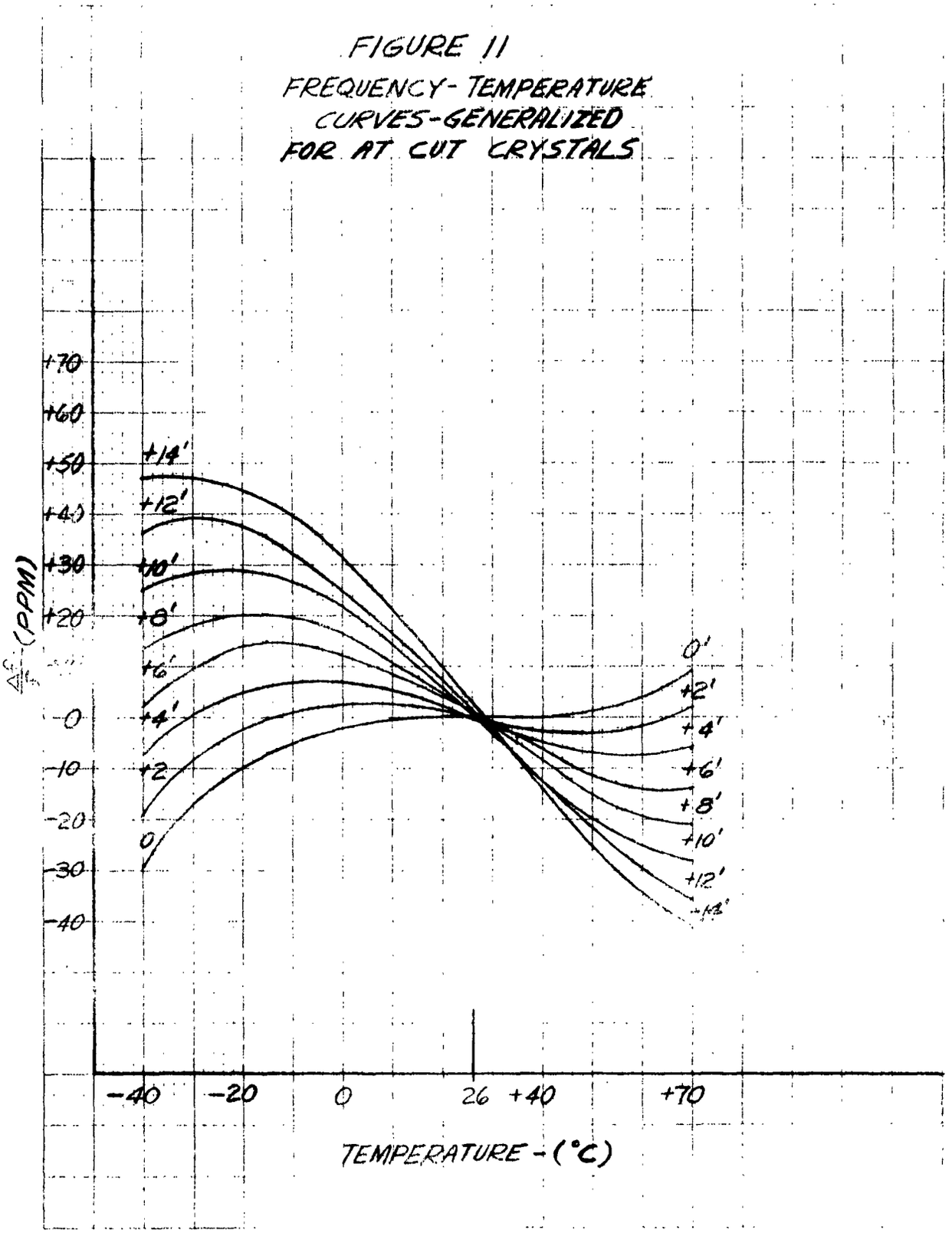
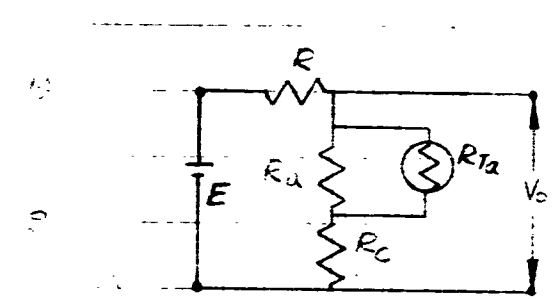
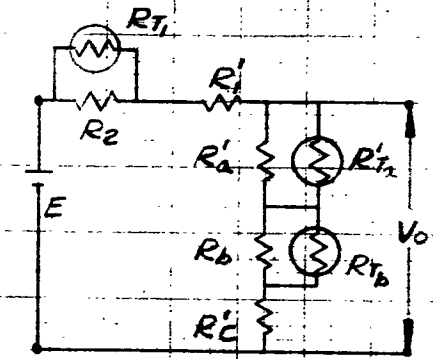


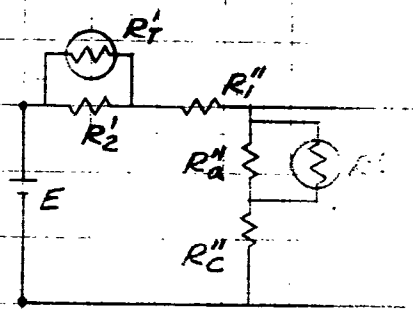
FIGURE 12
REQUIRED COMPENSATION VOLTAGE VS TEMPERATURE
AS A FUNCTION OF CRYSTAL ANGLE OF C·T FOR VARICAP COMPENSATION METHOD



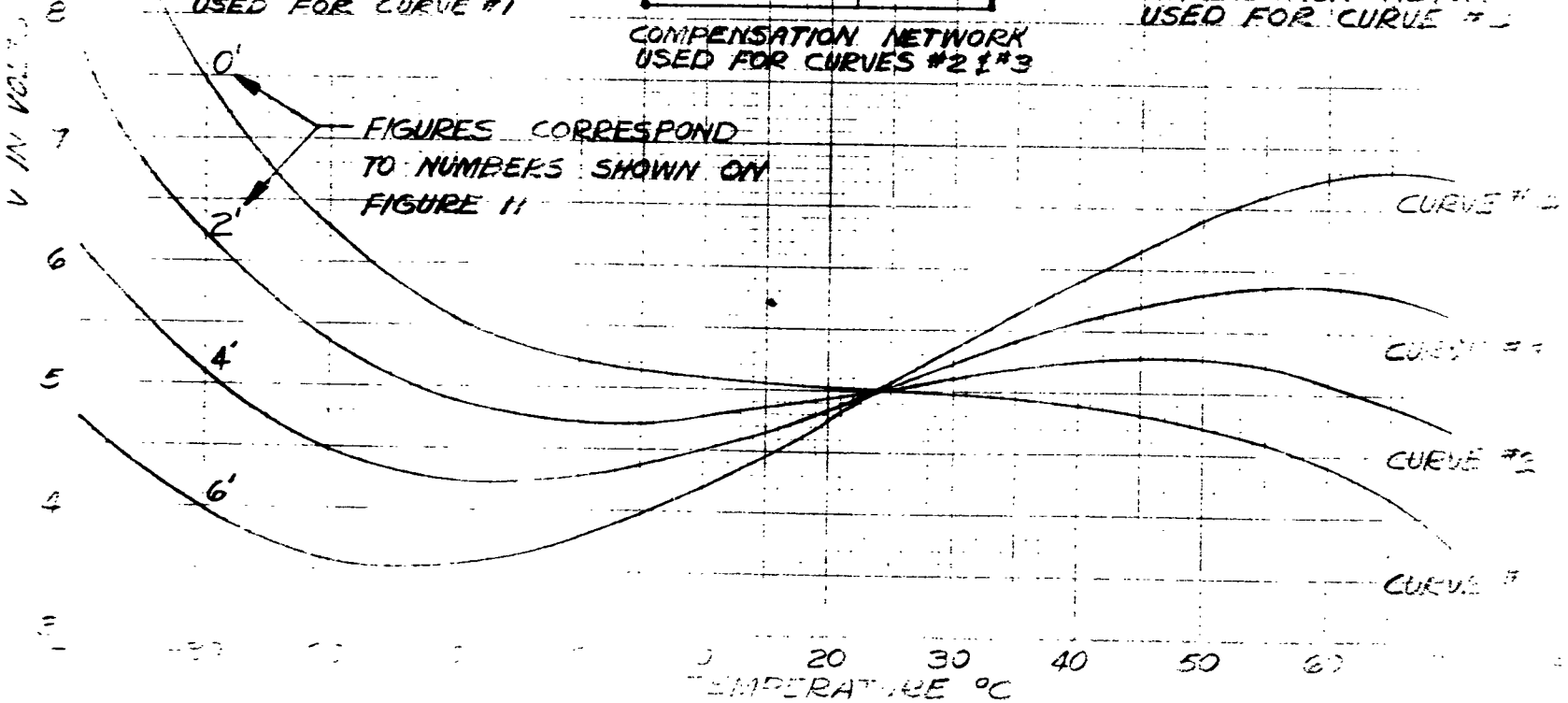
COMPENSATION NETWORK USED FOR CURVE #1



COMPENSATION NETWORK USED FOR CURVES #2 & #3



COMPENSATION NETWORK USED FOR CURVE #



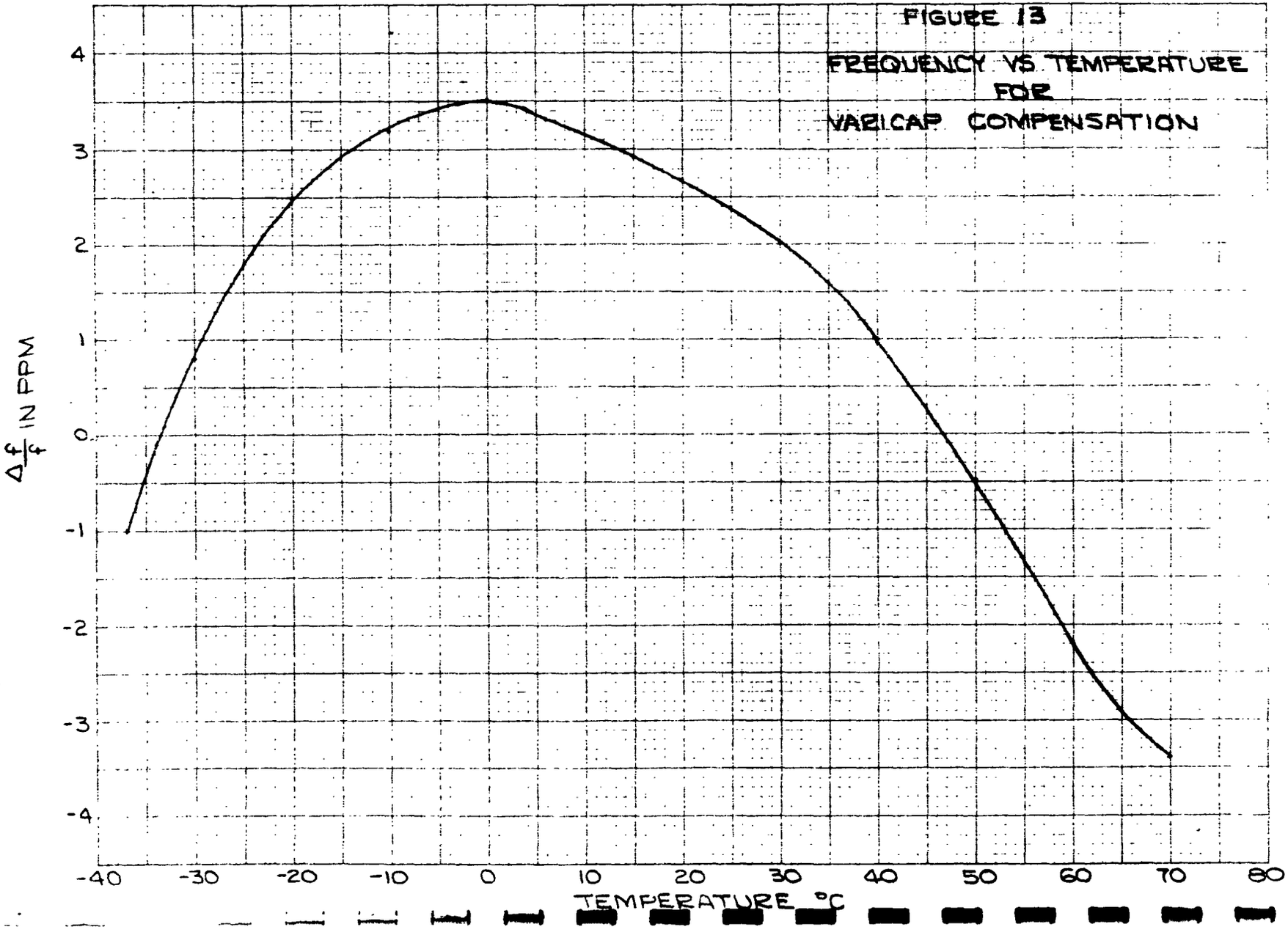


FIGURE 13
FREQUENCY VS TEMPERATURE
FOR
VARICAP COMPENSATION
$\frac{\Delta f}{f}$ IN PPM
4
3
2
1
0
-1
-2
-3
-4
-40
-30
-20
-10
0
10
20
30
40
50
60
70
80
TEMPERATURE °C

4.3 Transistor Compensation Method: Mathematical Analysis

The transistor method of compensation is based upon the junction capacitance of the oscillator transistor and its control. Figure 14a is the basic oscillator circuit used in investigating this method of compensation where R_1 and R_2 are variable resistances Figure 14b is the a-c equivalent circuit for Figure 14a. C_{cb} is the internal base to collector junction capacitance of the transistor. The junction capacitance is determined by the voltage from collector to base.

A mathematical analysis of the transistor compensation method has been made. Figure 15a is a schematic of the d-c portion of a transistor compensated oscillator and in Figure 15b the transistor is replaced with its simplified equivalent circuit where the base and emitter resistance is considered to be negligible.

The analysis of this circuit was made using V_{cb} as the parameter desired to be investigated. Using V_{cb} as the control parameter is mathematically simpler than using C_{cb} as the controlled parameter and just as effective because C_{cb} is proportional to V_{cb} as shown in Equation (1).

(1) $$C_{cb} = \frac{K}{V_{cb}^{n}} = \frac{K}{\sqrt{V_{cb}}}$$

All equations obtained in the following derivations can be related to C_{cb} by using Equations (1) and (11)

(2) $$I_c = BI_b + (B + 1)\ I_{co}$$

(3) $$I_c = I_e - I_b$$

(4) $$I_1 = I_2 + I_b$$

(5) $$E = R_1I_1 + R_2I_2$$

(6) $$I_eR_e = I_2R_2$$

(7) $V_{cb} = I_1R_1 - I_cR_c$

(8) $V_{cb} = I_b\left[\frac{R_1R_e}{R_2}(1 + B) + (R_1 - BR_c)\right] + I_{co}(B + 1)\left(\frac{R_eR_1}{R2} - R_c\right)$

From these equations, Equation (8) can be rewritten in terms of known parameters as shown in Equation (9) where $R_t = \frac{R_1R_2}{R_1 + R_2}$

(9) $V_{cb} = E\left[\frac{R_tB}{R_2(B+R_t/R_e)} + \frac{R_t}{R_e(B+R_t/R_e)} - \frac{BR_c}{R_e(1+R_1/R_2)(B+R_t/R_e)}\right]$

$+ I_{co}\left[\frac{BR_1R_e}{R_2} - R_c - \frac{B^2R_eR_1/R_2}{B+R_t/R_e} - \frac{(BR1+B^2R_c)}{B+R_t/R_e}\right]$

Neglecting I_{co}, Equation (9) reduces to Equation (10)

(10) $V_{cb} = E\left(\frac{R_1R_2}{R_1(B+R_2/R_e)+BR_2}\right)\left(B/R_2 + 1/R_e - BR_c/R_eR_1\right)$

By taking the derivative of V_{cb} with respect to the circuit parameters to be considered, Equations (11) through (17) are obtained.

(11) $\frac{dC}{dV_b} = -\frac{K}{2}V^{-3/2}$

(12) $\frac{dV_{cb}}{dE} = \left(\frac{R_1R_2}{B(R_1+R_2) + R_1R_2/R_e}\right)\left(B/R_2 + 1/R_e - BR_c/R_eR_1\right)$

(13) $\frac{dV_{cb}}{dR_1} = \frac{ER_2B(B + R_2 + BR_c/R_e + R_2R_c/R_e^2)}{(R_1(B + R_2/R_e) + BR_2)^2}$

(14) $\frac{dV_{cb}}{dR_2} = -\frac{EB^2(R_1 + R_1R_c/R_e)}{(BR_1 + R_2(B + R_1/R_c))^2}$

(15) $\frac{dV_{cb}}{dR_e} = \frac{EBR_1R_2\left[(R_1/(R_1+R_2) - 1 + (B(R_1+R_2)R_c)/(R_1R_2(1 + R_1/R_2))\right]}{(R_1 + R_2)(BR_e + R_1R_2/R_1+R_2)^2}$

$$(16)\qquad \frac{dV_{cb}}{dR_c} = -\frac{EB\,R_2}{R_1(R_2 + B\,R_e) + R_2R_eB}$$

$$(17)\qquad \frac{dV_{cb}}{dR_c} = \frac{E\,R_1R_2}{R_e(R_1 + R_2)\left(B + \frac{R_1R_2}{R_1 + R_2}\right)^2}\left(\frac{R_1}{R_1 + R_2} + 1 - \frac{R_c}{R_e\,(1 + \frac{R_1}{R_2})}\right)$$

Thus, by knowing a given change in circuit parameters, the resulting change in V_{cb} can be found and correlated to the resulting change in C_{cb} through Equation (11). As can be seen from the equations just derived, beta is a predominant factor. If beta can be made so large that $I_b << I_1$) then the previous equations can be rewritten using this assumption. The following equation was derived from Equation (10) assuming beta to be very large.

$$(18)\qquad \lim_{B \to \infty} V_{cb} = E\left[\frac{R_1}{R_1 + R_2} - \frac{R_c\,R_2}{R_e\,(R_1 + R_2)}\right] = E\left[\frac{R_e\,R_1 - R_c\,R_2}{R_e\,(R_1 + R_2)}\right]$$

Thus V_{cb} is determined by I_1 or I_2 and I_c or I_e or by R_1, R_2, R_c, or R_e. As was indicated in the previous analysis, this independence of P or V_{cb} on the beta of a compensated oscillator transistor would allow all compensation curves to be run at room temperature because the temperature effect of beta would be eliminated. In the case where beta is very large, the the Equations (12) through (17) reduce to the following set of equations:

$$(19)\qquad \frac{dV_{cb}}{dE} \doteq \frac{(R_1R_e - R_cR_2)}{R_1R_e + R_2R_e + R_1R_2}$$

$$(20)\qquad \frac{dV_{cb}}{dR_1} \doteq E\left(\frac{R_2}{R_e}\right)\frac{(R_e + R_c)}{(R_1 + R_2)^2}$$

$$(21)\qquad \frac{dV_{cb}}{dR_2} \doteq -\left(\frac{E}{R_e}\right)\frac{(R_1R_e + R_1R_c)}{(R_1 + R_2)^2}$$

$$(22)\qquad \frac{dV_{cb}}{dR_e} \doteq E\,\frac{E\,R_2R_c}{R_e^{\,2}\,(R_1 + R_2)}$$

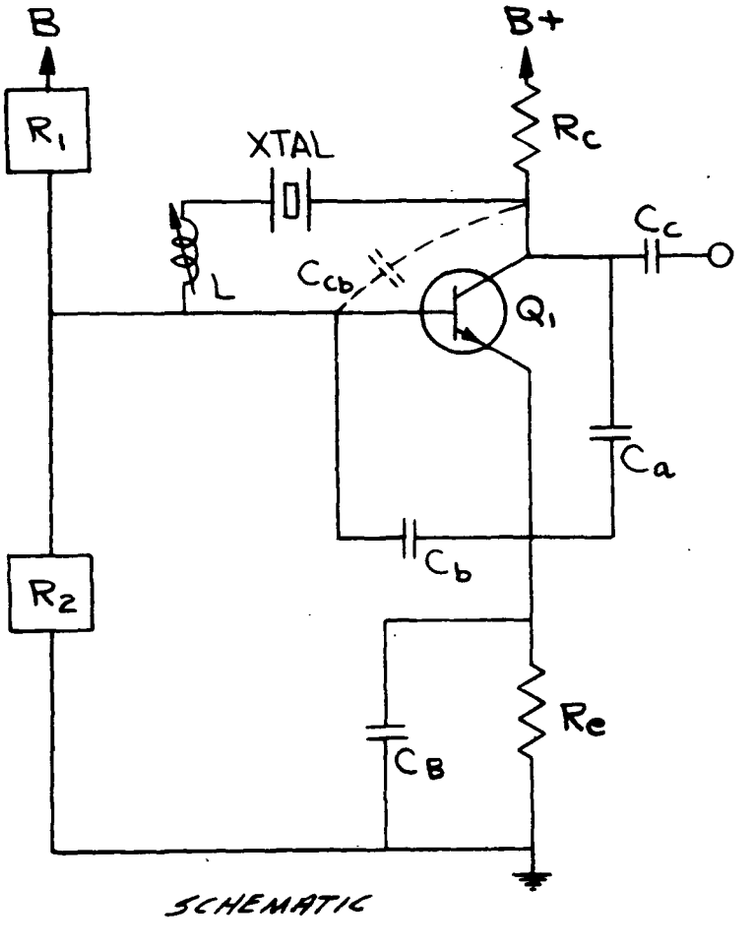
$$(23)\qquad \frac{dV_{cb}}{dR_c} \doteq -\,\frac{E\,R_2}{R_e\,(R_1 + R_2)}$$

$$(24)\qquad \frac{dV_{cb}}{dB} \doteq 0$$

It is apparent from the above equations that if beta is large enough to be ignored, then its temperature variations can also be ignored. This greatly reduces the complexity of the equations governing the transistor compensation method.

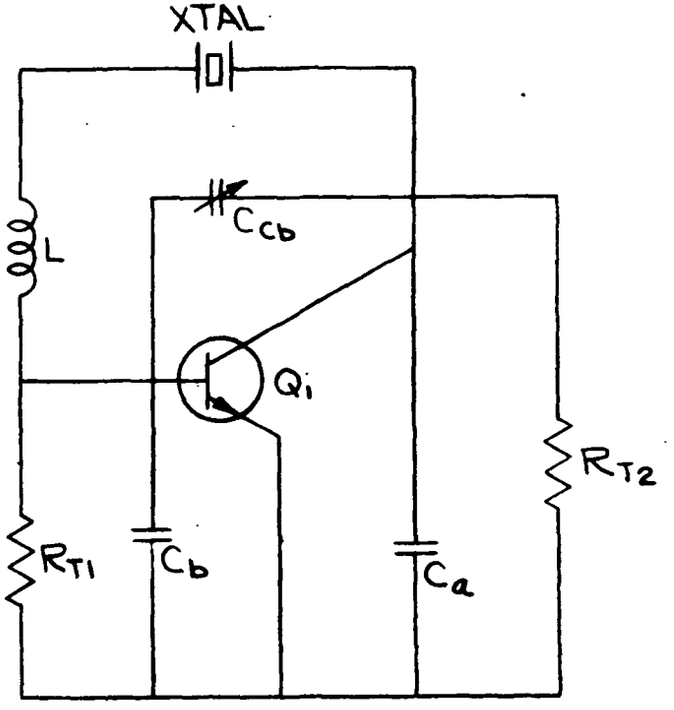
Therefore, the change in C_{cb} with a change in any circuit resistance, particularly R_1 and R_2, can be determined very readily. This in turn can be related to a change in frequency for a change in R_1 and R_2 by obtaining the equivalent circuit of the transistor compensated oscillator and solving for P as a function of C_{cb} of R_1 and R_2.

In actuality, beta large enough to have no effect on the transistor compensation equation will never be achieved, but beta may be large enough that Equation (18) will be very close approximation for V_{cb}. At the present time, an investigation is being conducted to find transistors with higher betas than those now being used or a method of increasing the effective beta of the transistor.



SCHEMATIC

(a)



A-C EQUIVALENT CIRCUIT

(b)

TRANSISTOR COMPENSATION CIRCUIT

FIGURE 14

EQUIVALENT D.C. CIRCUITS

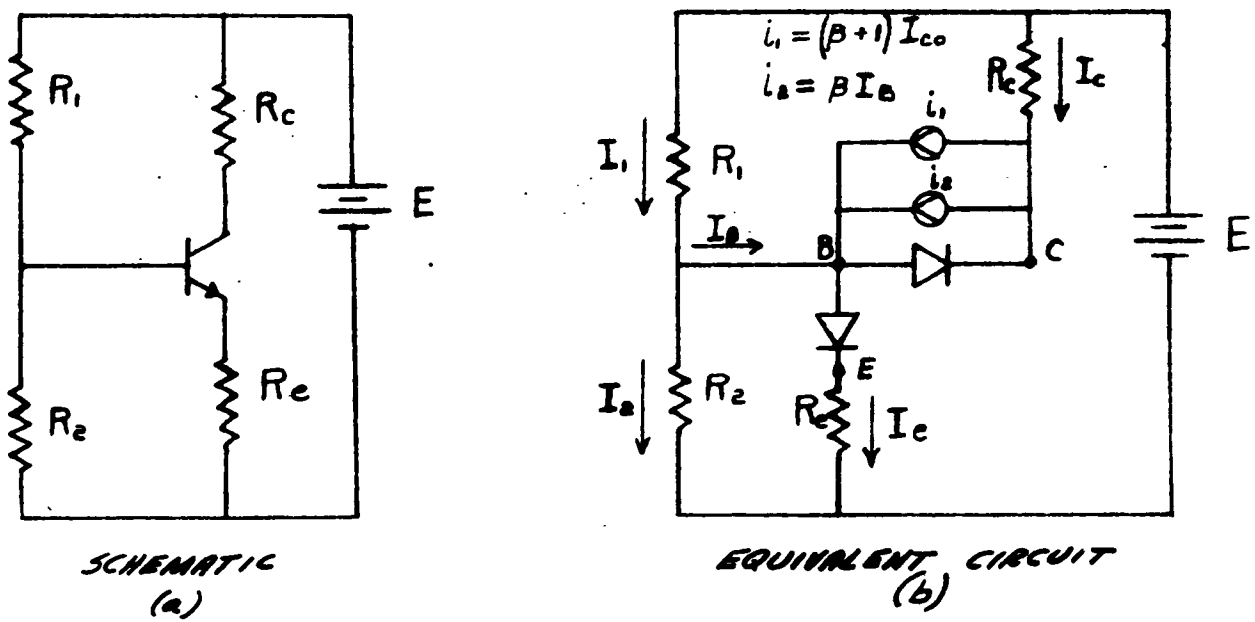


FIG. 15

4.4 Transistor Compensation Method: Empirical Data

The basic circuit used in investigating the transistor compensation method was shown in Figure 14a. The configuration of the oscillator is fixed in this study to oscillators such as those shown in Figure 16. In any oscillator using the transistor method, the junction capacity C_{cb} must be in such a position that it can control the frequency of the oscillator. This requires that the junction capacity in circuit (a) in Figure 16 appear across the inductance and crystal, in circuit (b) from base to ground or in circuit (c) from collector to ground. Configuration (b) requires that the collector be grounded. The configuration in (c) requires that the base be grounded. All three configurations have been tried. There is no advantage in grounding the collector as in configuration (b), unless it is desired to have one side of the crystal grounded. The reason for grounding the base is to eliminate any effects that varying R_1 and R_2 might have on the frequency of the oscillator.

The relationship between R_1 and R_2 and P has been investigated. This relationship is basically the same for all transistors. The value of junction capacitance and the change in capacitance with junction voltage of a given transistor determines the magnitude of the effect of R_1 and R_2 on frequency. At three megacycles the reactance change required to obtain adequate pullability requires a junction capacitance of approximately 20 to 30 uf. This requirement immediately rules out a large number of high frequency transistors because of their low junction capacity. During the experiments performed the 2N697 transistor was used almost exclusively because it meets the requirements of good frequency characteristics and large junction capacity. Other transistors were used and a comparison to the 2N697 of a 2N1507 is given in Figure 17. A very high gain, large capacitance transistor is now on order that should have a much higher beta than the 2N697.

There is a difference in the slope of the $\Delta f/f$ versus R curves for various transistors. The transistors used in the experiments were not selected for uniformity. If they had been selected according to junction capacity, more uniform characteristics would have been obtained. The curves of R_1 and R_2 versus P indicate that the change

in resistance of R_1 will slightly affect the pullability of R_2 and R_2 will affect the pullability of R_1. This is true because of the change in base current in the compensation network.

Temperature also has some effect on the slope of the R versus P curves. Most of this effect is due to the change in beta of the transistor with temperature. A high gain transistor will eliminate most of the temperature dependence of the pullability $\Delta P/\Delta R$.

The general curves of R_1 and R_2 versus temperature required to compensate a crysta show similar characteristics to those of curves (a) and (b) in Figure 18. This curve is true if it is assumed only NTC thermistorsare used for compensation. If both positive and negative coefficient thermistors are used it is possible to use only R_1 for the compensation element. A typical compensation curve of R_1 using both PTC and NTC thermistors is shown in Curve (c). Although the use of only R_1 for compensation greatly simplifies the compensation procedure, PTC thermistors are not available in enough of a variety to obtain the flexibility in compensation characteristics required. Therefore, almost all of the experiments performed on transistor compensated oscillators was done using both R_1 and R_2 to generate the $\Delta f/f$ versus temperature characteristics. R_1 essentially controls the low temperature compensation requirements and R_2 controls the high temperature requirements. There is a certain amount of interaction between R_1 and R_2 at the intermediate temperatures. Figure 19 shows an ideal case where R_1 becomes ineffective at T_2, and R_2 becomes effective at T . Methods whereby the resistance changes in R_1 do not affect the compensation performed by R_2 and resistance changes in R_2 do not affect the compensation provided by R_1 are being investigated and will be discussed in the section on non-linear resistance networks.

Four oscillators have been compensated to varying degrees of accuracy using the transistor method. Figure 20 shows the circuit for the four oscillators and also gives the uncompensated change in frequency between turning points for each oscillator. Figure 21 gives the resulting curves for Oscillators #1 and 2. Figures 22 and 24 show the evolution of the final frequency versus temperature curve from the original

uncompensated oscillator curve for Oscillators #3 and 4. Figures 23 and 25 show the circuits for the R_1 and R_2 for each curve in Figures 22 and 24.

Oscillator #1 and 3 utilize the grounded emitter configuration and Oscillator #2 and 4 utilize the grounded base configuration. From Figures 21, 22, and 24 it is quite apparent that the oscillators using the grounded emitter configuration were more successfully compensated. During the compensation procedure, it was determined that $\Delta P/PR$ for the grounded base configuration was less than for the grounded emitter configuration. Initially, networks for R_1 and R_2 were devised from the R_1 and R_2 versus P of the oscillator that would compensate for the frequency change due to temperature. When the resulting curve was plotted from the data obtained on the first temperature run using the initial R_1 and R_2 networks, the error in frequency was plotted versus temperature. From the error curves, correction curves for R_1 and R_2 were then changed to incorporate the required error correcting resistance. This procedure was done until the errors became so small that further compensation was not feasible for the time required or until the effect of R_1 and R_2 were at their limits and no more compensation could be accomplished without major circuit changes.

The crystals used in the test oscillator were not optimum with respect to the Δf between turning points. They were all that were available at the time the program was started. Using crystals with less slope between turning points would require less compensation and, consequently, less frequency pulling capability. This would result in a fewer number of trial temperature runs to achieve a given frequency stability.

The change in frequency with a change in B+ was determined experimentally as shown in Figure 26. The average slope of the curves is approximately (0.6) PPM/volt. This indicates that to keep the effect of supply voltage variations or frequency to less than $\pm$ 0.01 PPM; the supply voltage cannot vary more than $\pm$.0167 volts.

To compensate an oscillator to less than $\pm$ 1 PPM using the transistor method will probably involve a change in compensation techniques. The variation in C_{cb} with voltage for a given number of transistors will vary unless transistors are selected. Therefore, it is hard to specify a thermistor-resistor circuit that will compensate an

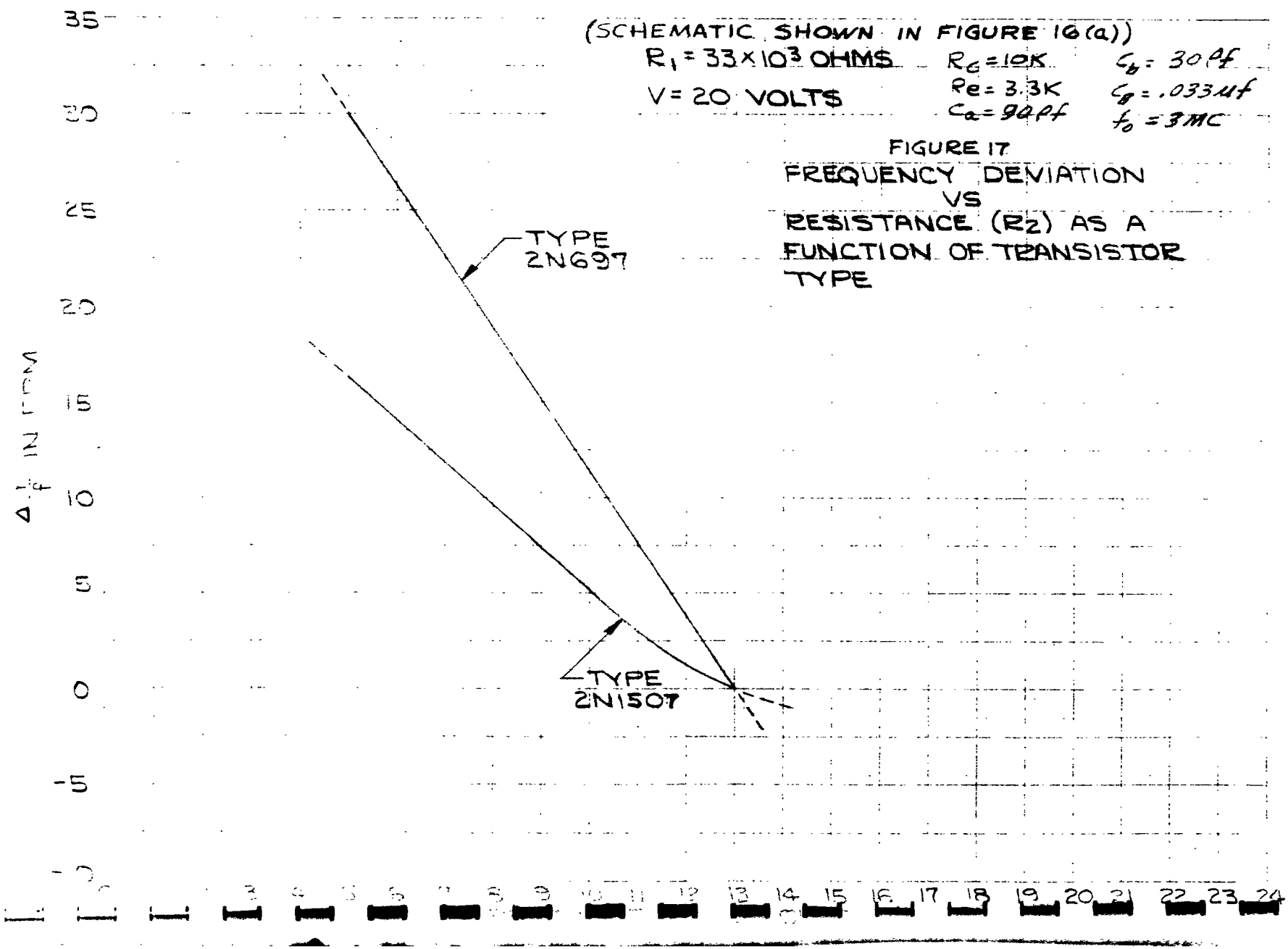
oscillator to very close [illegible] when different transistors are used. For accuracies below 1 PPM, one method to compensate an oscillator would be for each transistor to be individually checked and compared to previous transistors that had been used for compensation. In this way, transistors could be sorted into different categories and a specific compensation network could be used for each category.

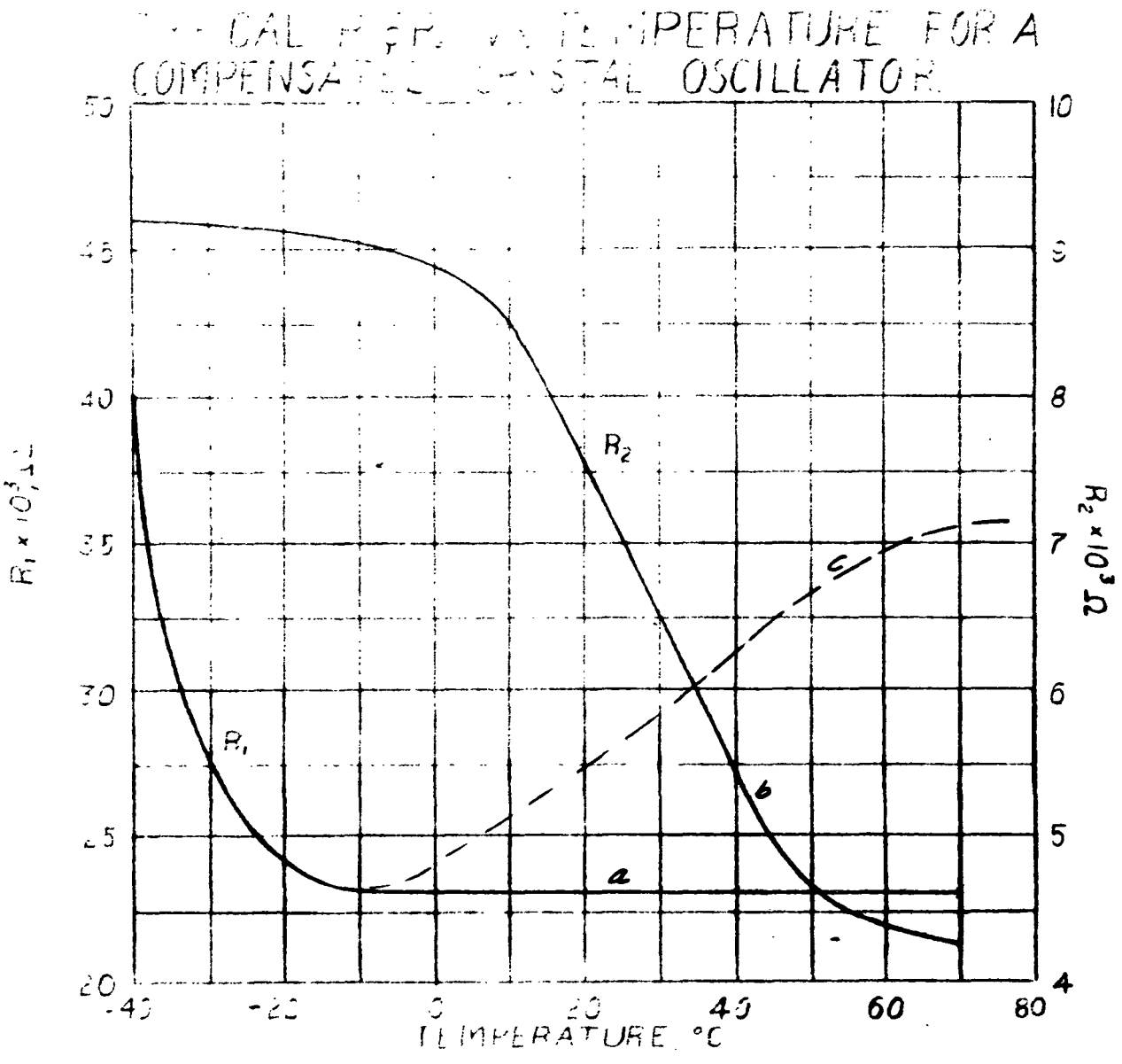
Another method that has been used to compensate an oscillator to frequency changes less than a PPM is the ΔR system. In the ΔR system a small resistor of known value is inserted in series with R_1 and R_2 with a shorting switch in parallel with the ΔR's. When a temperature run is made on the oscillator ΔR_1 and ΔR_2 are shorted at each temperature. The change in frequency for a change in R_1 and R_2 is recorded and plotted. This results in a plot of P versus temperature for a given ΔR_1 and ΔR_2. When the compensated $\Delta f/f$ versus temperature curve of the oscillator has been plotted, the error in frequency can be determined. From this the required change in R_1 and R_2 can be determined and the thermistor networks can be adjusted accordingly.

This method has been tried and works very satisfactorily but can become rather lengthy due to the fact that it is sometimes difficult to change the values of R_1 and R_2 by a given amount over a limited temperature range. In some cases, circuitry will have to be added to change the resistance versus temperature curve of R_1 and R_2 rather than changing the values already incorporated in R_1 and R_2. This may result in an excessive number of components if many changes are required to achieve the required frequency accuracy.

TRANSISTOR COMPENSATION METHOD

(b)


(SCHEMATIC SHOWN IN FIGURE 16(a))
$R_1 = 33 \times 10^3$ OHMS
V = 20 VOLTS
R_G = 10K
Re = 3.3K
C_a = 90Pf
C_b = 30Pf
C_g = .033uf
f_o = 3MC
FIGURE 17
FREQUENCY DEVIATION VS RESISTANCE (R_2) AS A FUNCTION OF TRANSISTOR TYPE
TYPE 2N697
TYPE 2N1507
$\frac{\Delta f}{f}$ IN PPM
35
30
25
20
15
10
5
0
-5
-10
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
22
23
24


CAL PERFORMANCE VS TEMPERATURE FOR A
COMPENSATED CRYSTAL OSCILLATOR
R1 x 10³, Ω
R2 x 10³, Ω
R1
R2
a
b
c
50
45
40
35
30
25
20
10
9
8
7
6
5
4
-40
-20
0
20
40
60
80
TEMPERATURE °C

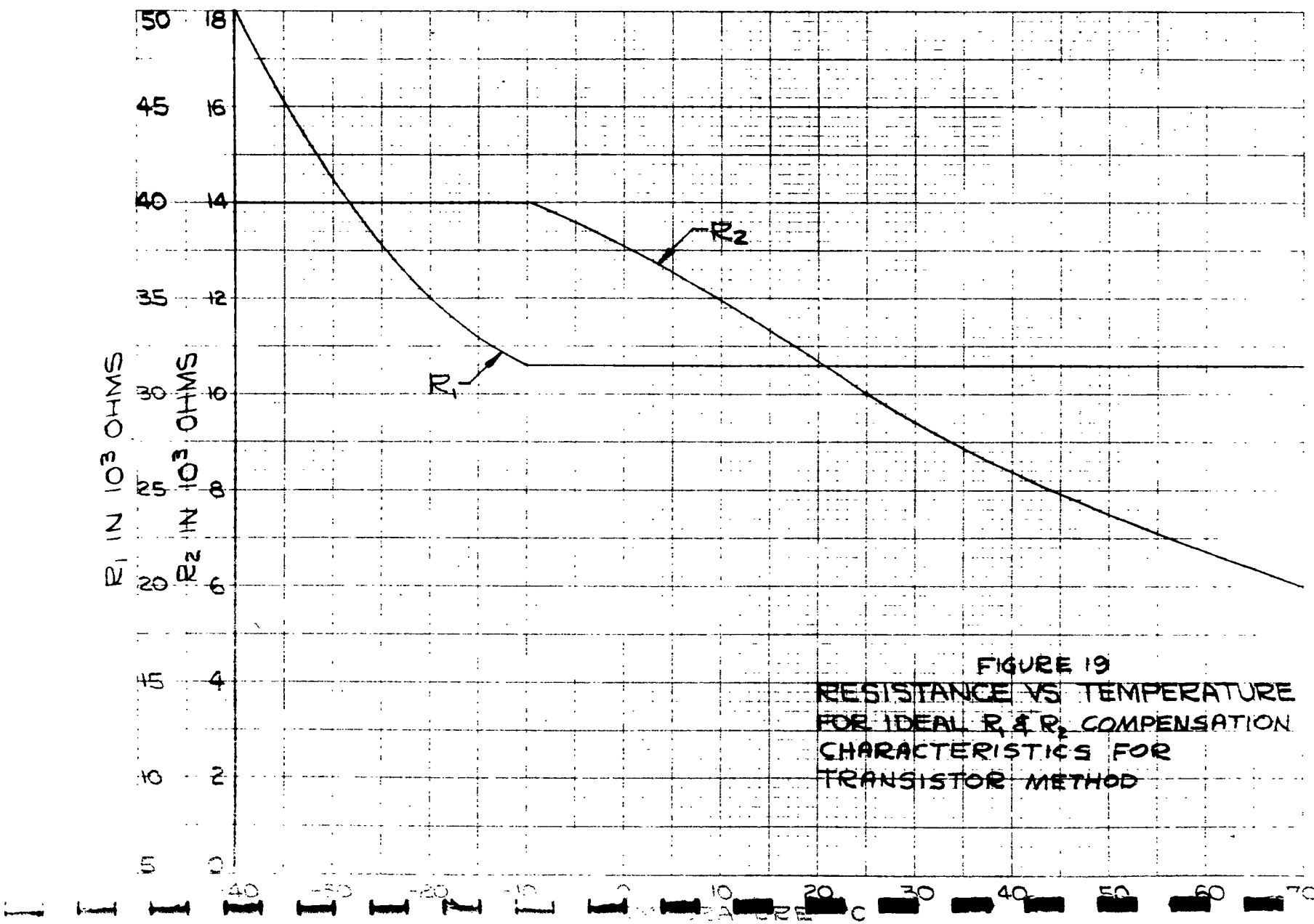
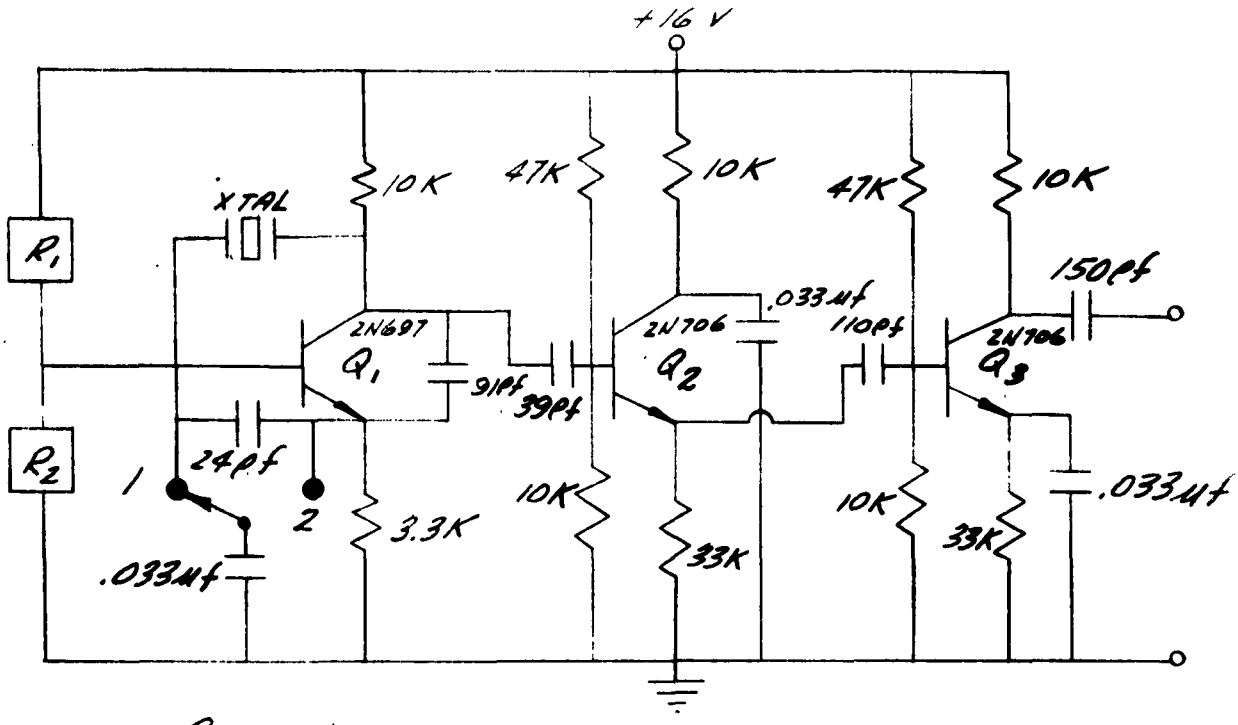


FIGURE 19
RESISTANCE VS TEMPERATURE FOR IDEAL R_1 & R_2 COMPENSATION CHARACTERISTICS FOR TRANSISTOR METHOD



Q_1 = 2N697

Q_2 = 2N706

Q_3 = 2N706

OSCILLATOR No.	S	f (Mc)	Δf (CYCLES)
1	2	3.707	142
2	1	3.707	144
3	2	3.637	68
4	1	3.637	78

S = SWITCH POSITION

f = CRYSTAL FREQUENCY

Δf = DIFFERENCE IN FREQUENCY FROM UPPER TO LOWER TURNING POINT

CIRCUIT DIAGRAM OF AGING OSCILLATOR

FIGURE 20

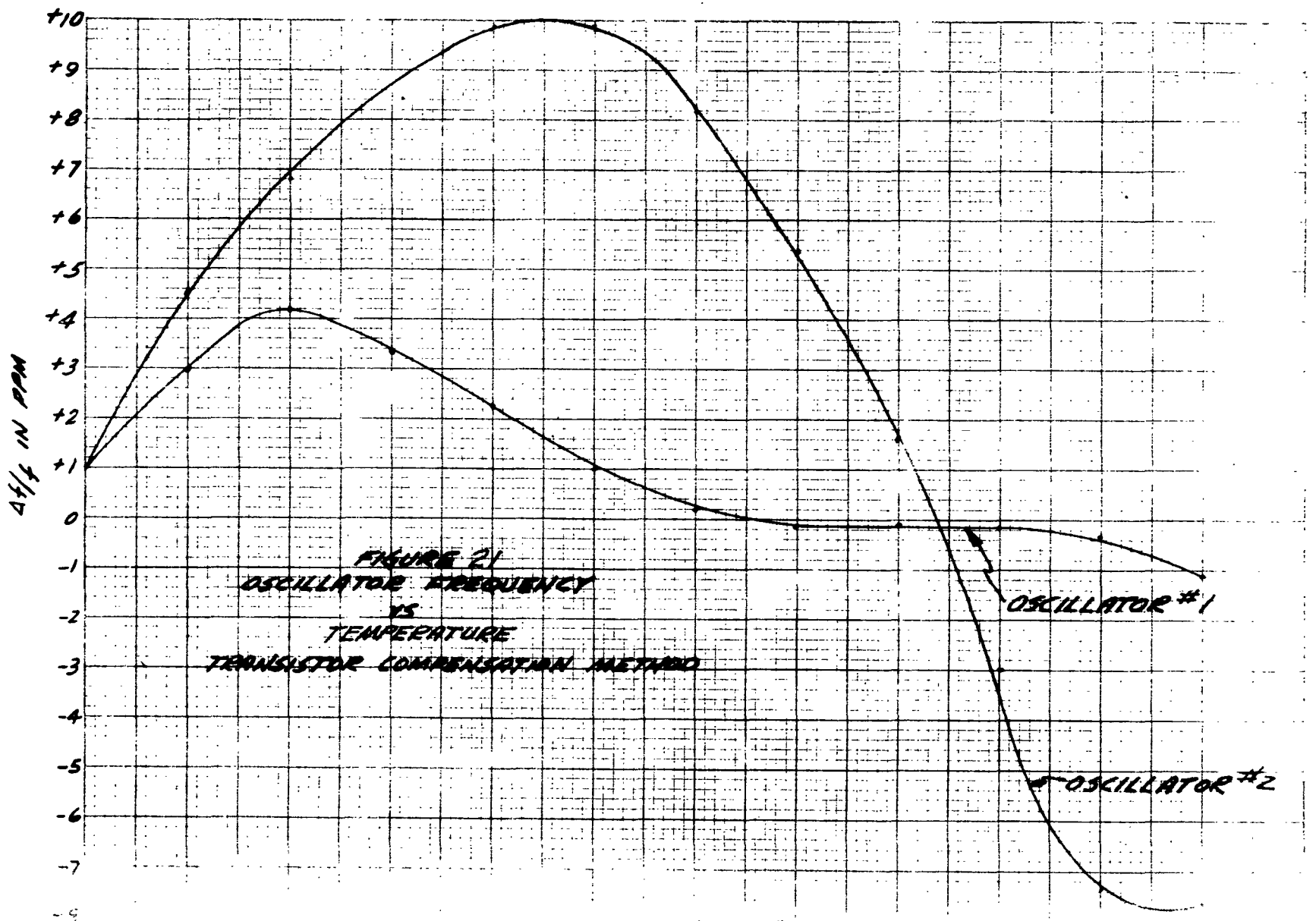


FIGURE 21
OSCILLATOR FREQUENCY
VS
TEMPERATURE
TRANSISTOR COMPENSATION METHOD

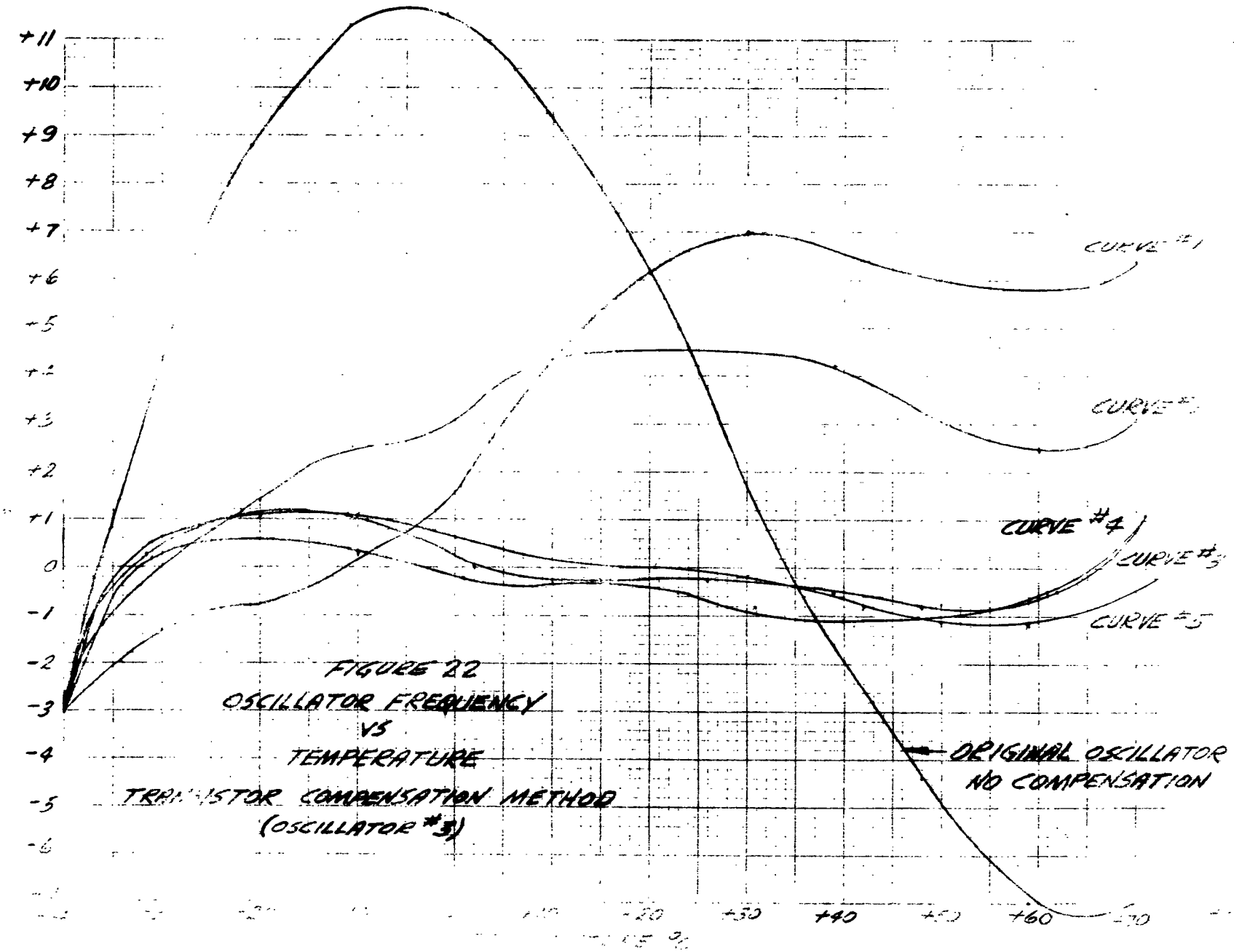
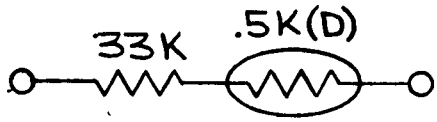
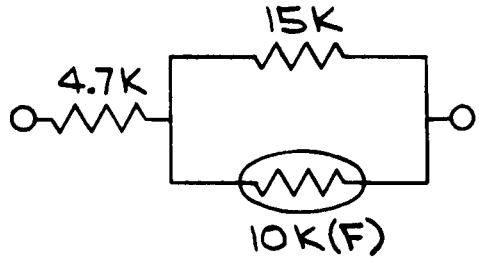
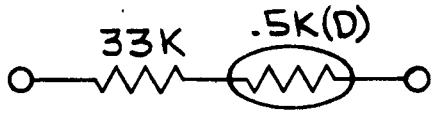
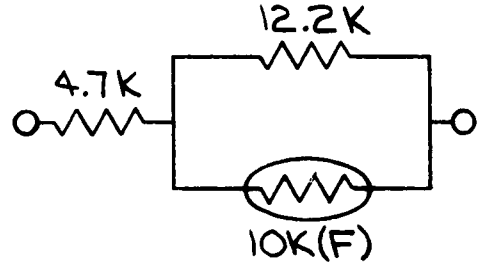
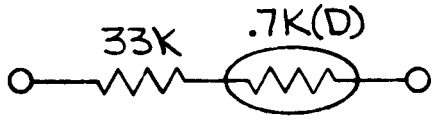
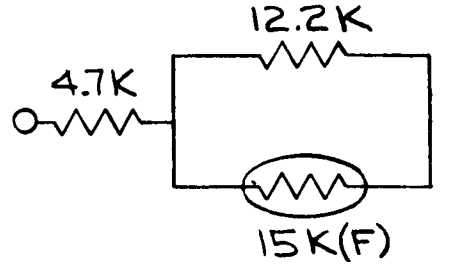
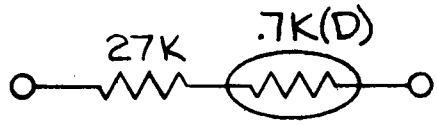
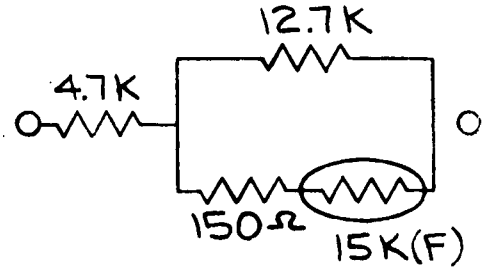
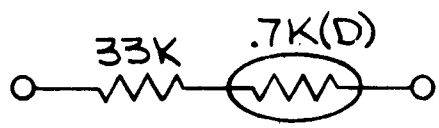
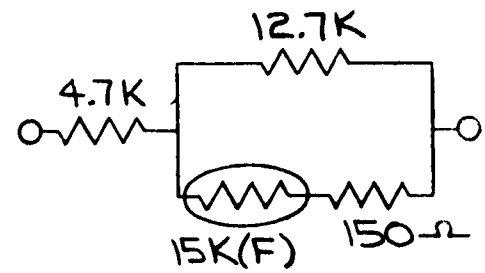


FIGURE 22
OSCILLATOR FREQUENCY
VS
TEMPERATURE
TRANSISTOR COMPENSATION METHOD
(OSCILLATOR #3)

OSCILLATOR #3

RUN NO.	R_1 ALL THERMISTORS GULTON TYPE(D)	R_2 ALL THERMISTORS GULTON TYPE(F)
1		
2		
3		
4		
5		

COMPENSATION NETWORKS
FIGURE 2.3

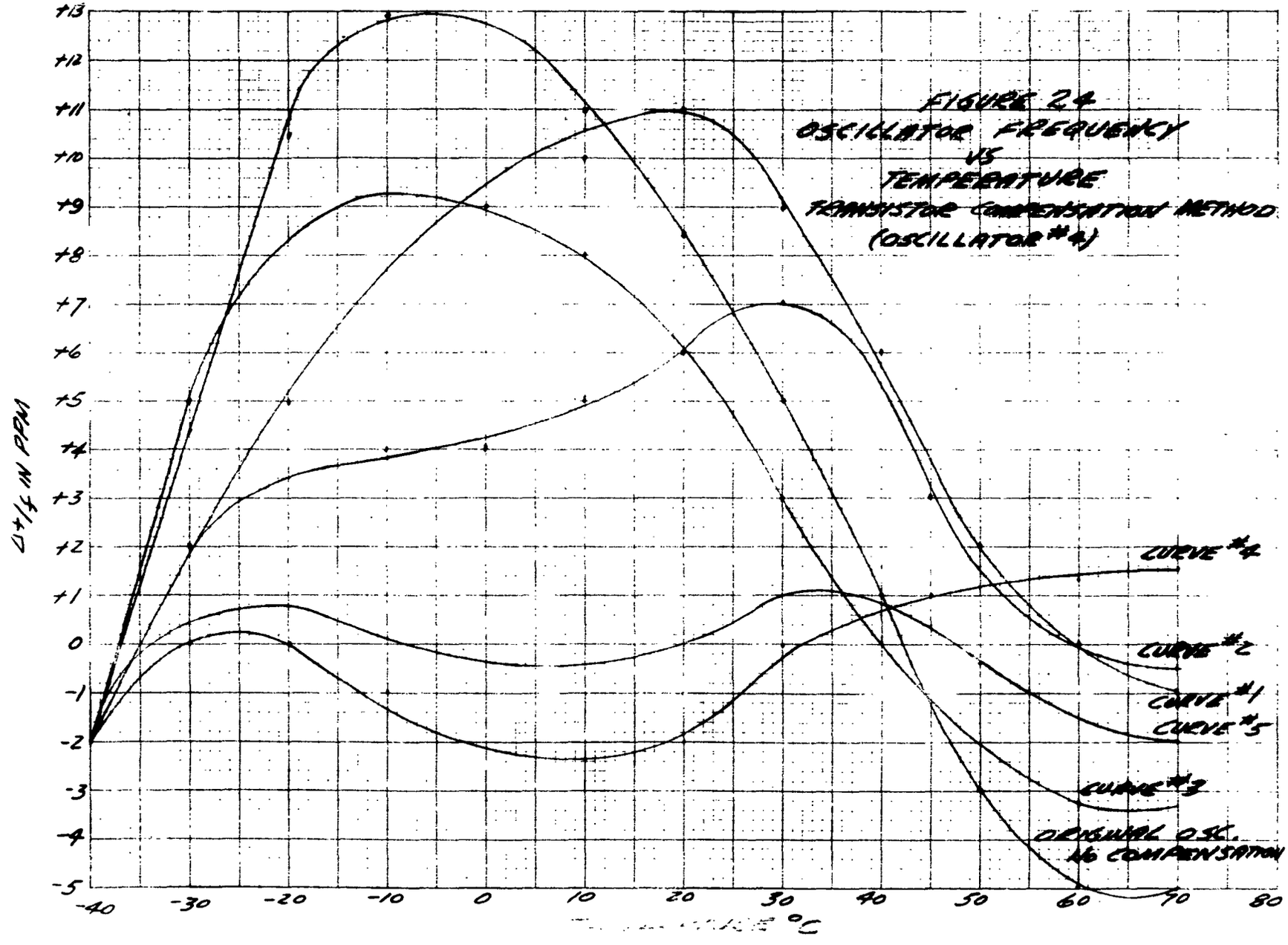
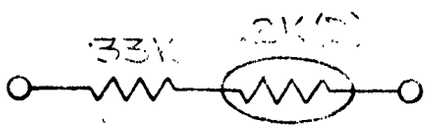
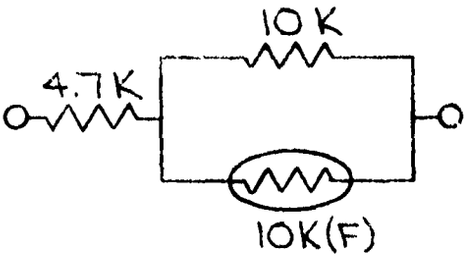
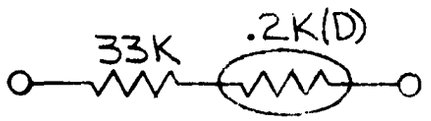
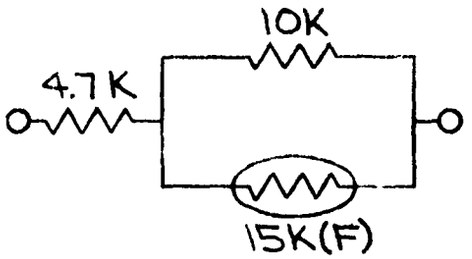
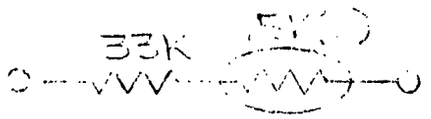
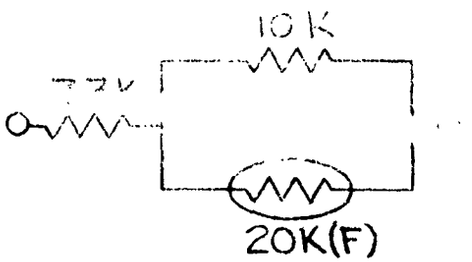
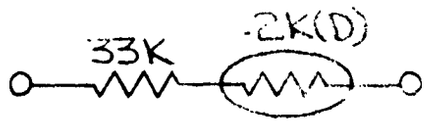
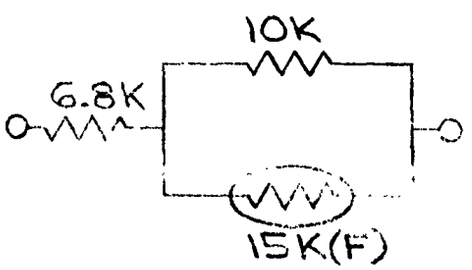
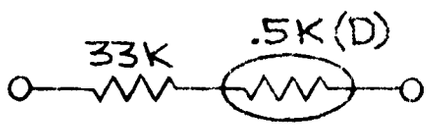
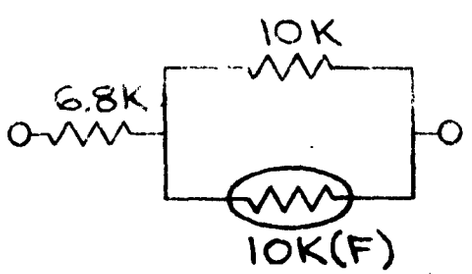


FIGURE 24
OSCILLATOR FREQUENCY
VS
TEMPERATURE
TRANSISTOR COMPENSATION METHOD
(OSCILLATOR #4)
CURVE #4
CURVE #2
CURVE #1
CURVE #5
CURVE #3
ORIGINAL O.S.C.
NO COMPENSATION
+13
+12
+11
+10
+9
+8
+7
+6
+5
+4
+3
+2
+1
0
-1
-2
-3
-4
-5
-40
-30
-20
-10
0
10
20
30
40
50
60
70
80
°C

OSCILLATOR #1

RUN NO.	R_1 GULTON TYPE (D)	R_2 ALL THERMISTORS GULTON TYPE (F)
1		
2		
3		
4		
5		

COMPENSATION NETWORKS
FIGURE 25

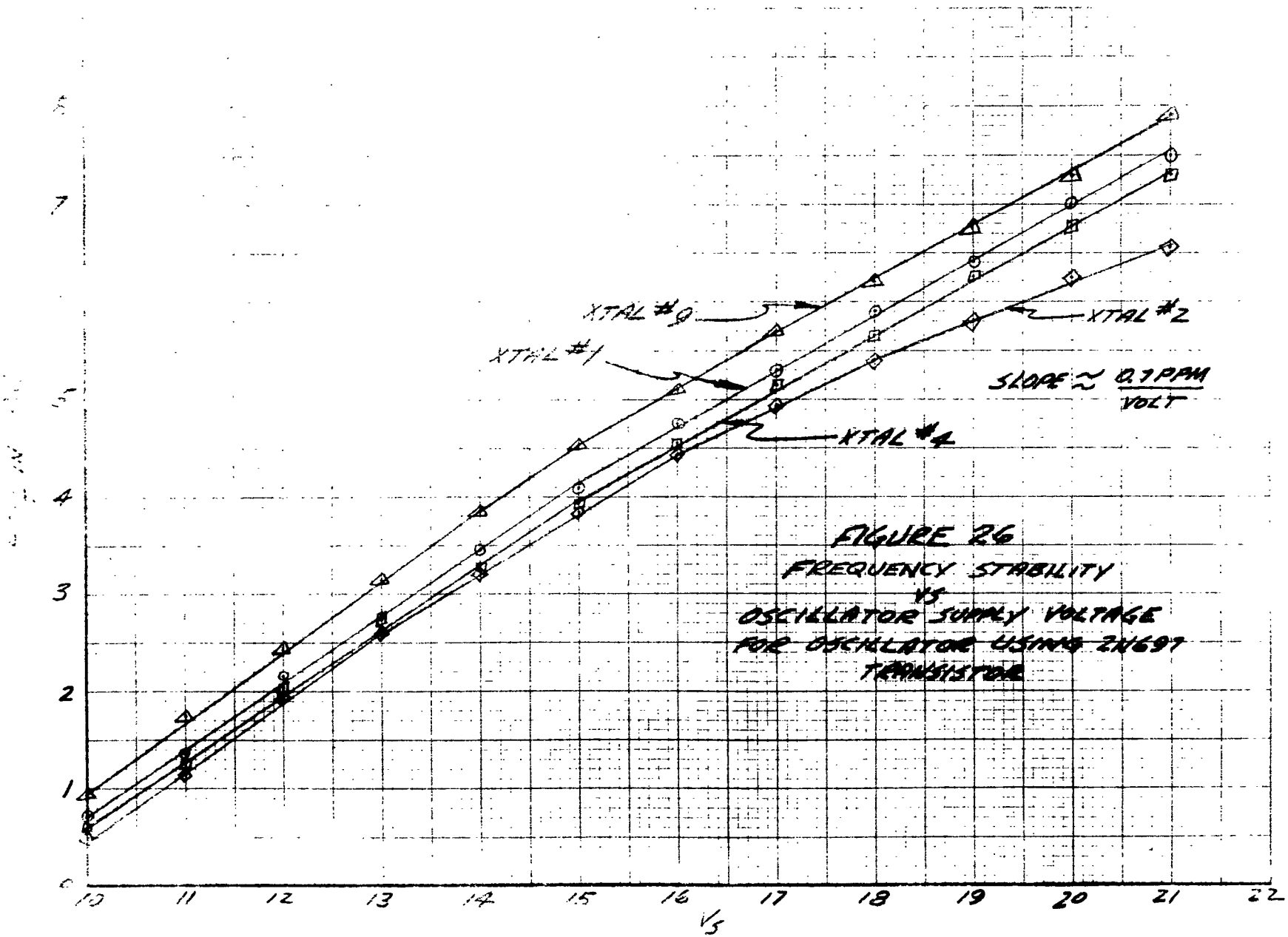


FIGURE 26
FREQUENCY STABILITY
VS
OSCILLATOR SUPPLY VOLTAGE
FOR OSCILLATOR USING 2N697
TRANSISTOR

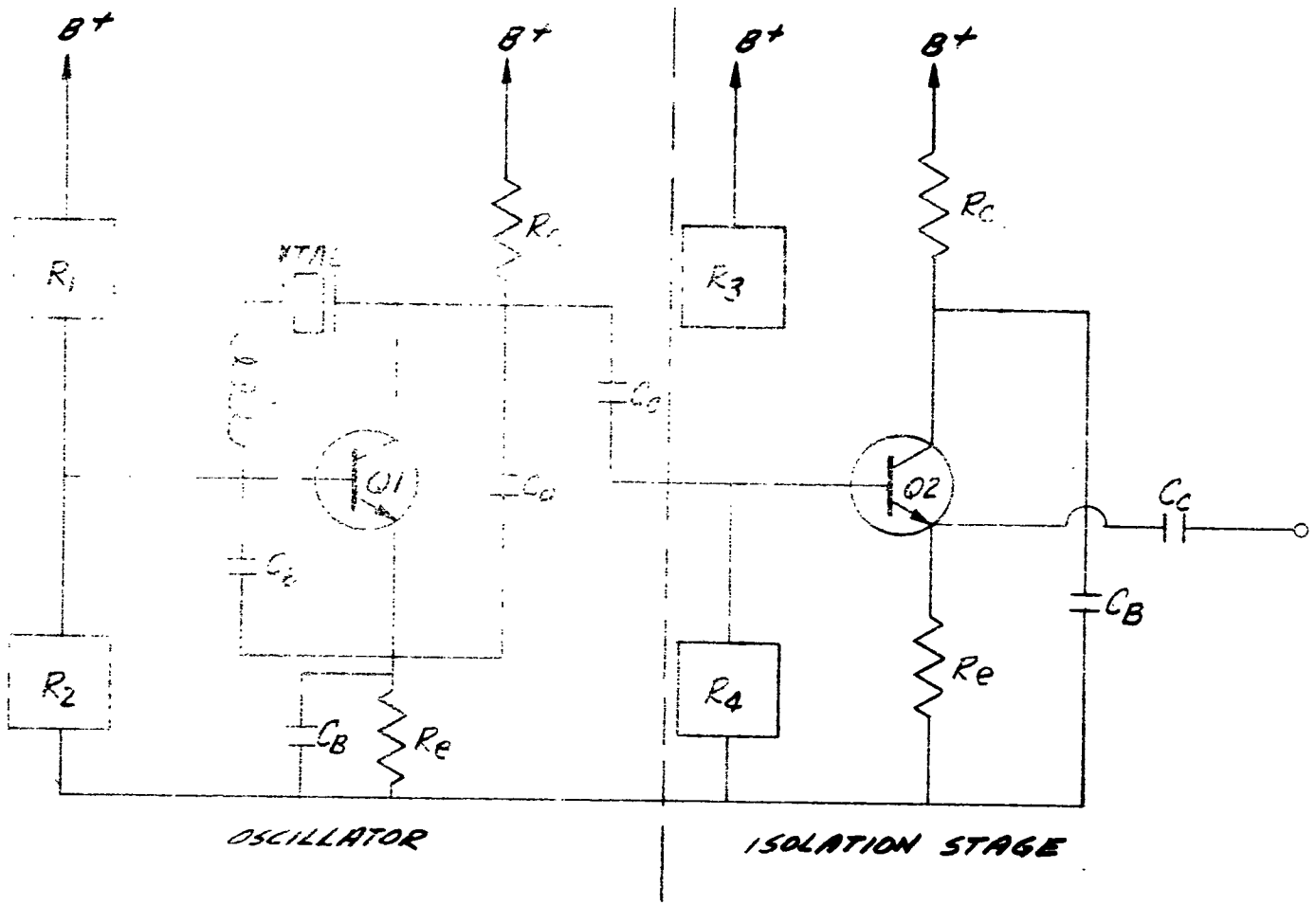
4.5 Isolation Stage Compensation

The isolation stage method of compensation utilizes the same principles as the transistor method of compensation, and the equations derived in the section of transistor compensation are good for System B'. This method was developed during a search for a means of providing a "fine" compensation control for the transistor method. By using the transistor and isolation stage methods together, compensation can effected much more readily. Figure 27 is a schematic of an oscillator utilizing the isolation stage compensation method.

The isolation stage method of compensation is most effective when the transistor method is used to reduce the frequency deviation of the oscillator with temperature with a standard compensation network. The error in frequency that still remains is then corrected for by using the transistor in the isolation stage for compensation, which will have less effect on the frequency than the oscillator transistor. This in effect provides a "fine" compensation adjustment where the oscillator transistor provides a "coarse" frequency adjustment.

Figures 28 and 29 are curves of P versus R_2 as a function of R_3, R_4 and C_c are as shown in the schematic in Figure 27. Figures 28 and 29 illustrate the effect of R_1, R_2 and R_4 upon the compensation characteristics of the isolation stage method. To illustrate, the slope of Curve #1 in Figure 28 is equal to $\Delta P/\Delta R_2$; the difference in $\Delta f/f$ between Curves #1 and #2 is equal to $\Delta P/\Delta R_4$, the difference in $\Delta f/f$ between Curves #1 and #3 is equal to $\Delta P/\Delta R_1$. The coupling capacitor, C_c, determines the magnitude of the effect that the change in junction capacitance of the isolation stage transistor has on the frequency output of the oscillator. The effect of changing C_c is shown in Figure 29. C_c is therefore a control on the pullability that the isolation stage transistor exhibits. Data was also taken on the effect of changing the load on the isolation stage when it is used for compensation. The effect on frequency for a reasonable change in load was not detectable. The plot of P versus R_2 as a function of R_1 and R_4 was made to get an order of magnitude effect of change in frequency for a change in the various compensation resistances.

Using the isolation ... compensation method, an oscillator has been compensated to a certain degree as shown in Figure 30. This compensation curve was made using only the isolation stage transistor; the bias on the oscillator transistor was fixed.



OSCILLATOR INCORPORATING OSCILLATOR TRANSISTOR AND ISOLATION STAGE COMPENSATION METHODS

FIGURE 27

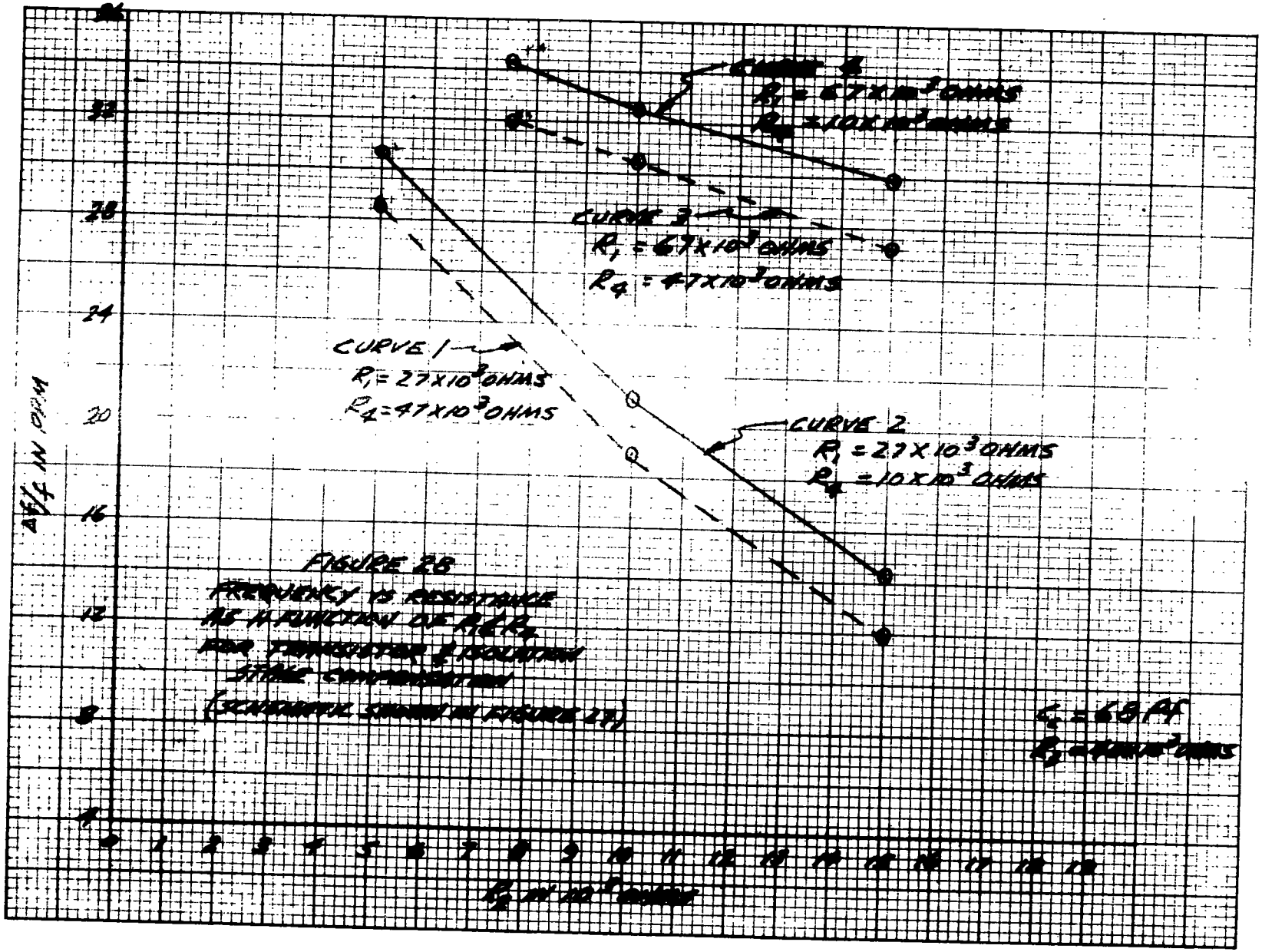


FIGURE 28
FREQUENCY VS RESISTANCE
AS A FUNCTION OF R_1 & R_4
FOR TEMPERATURE COMPENSATED
STABLE OSCILLATOR
(SCHEMATIC SHOWN IN FIGURE 27)

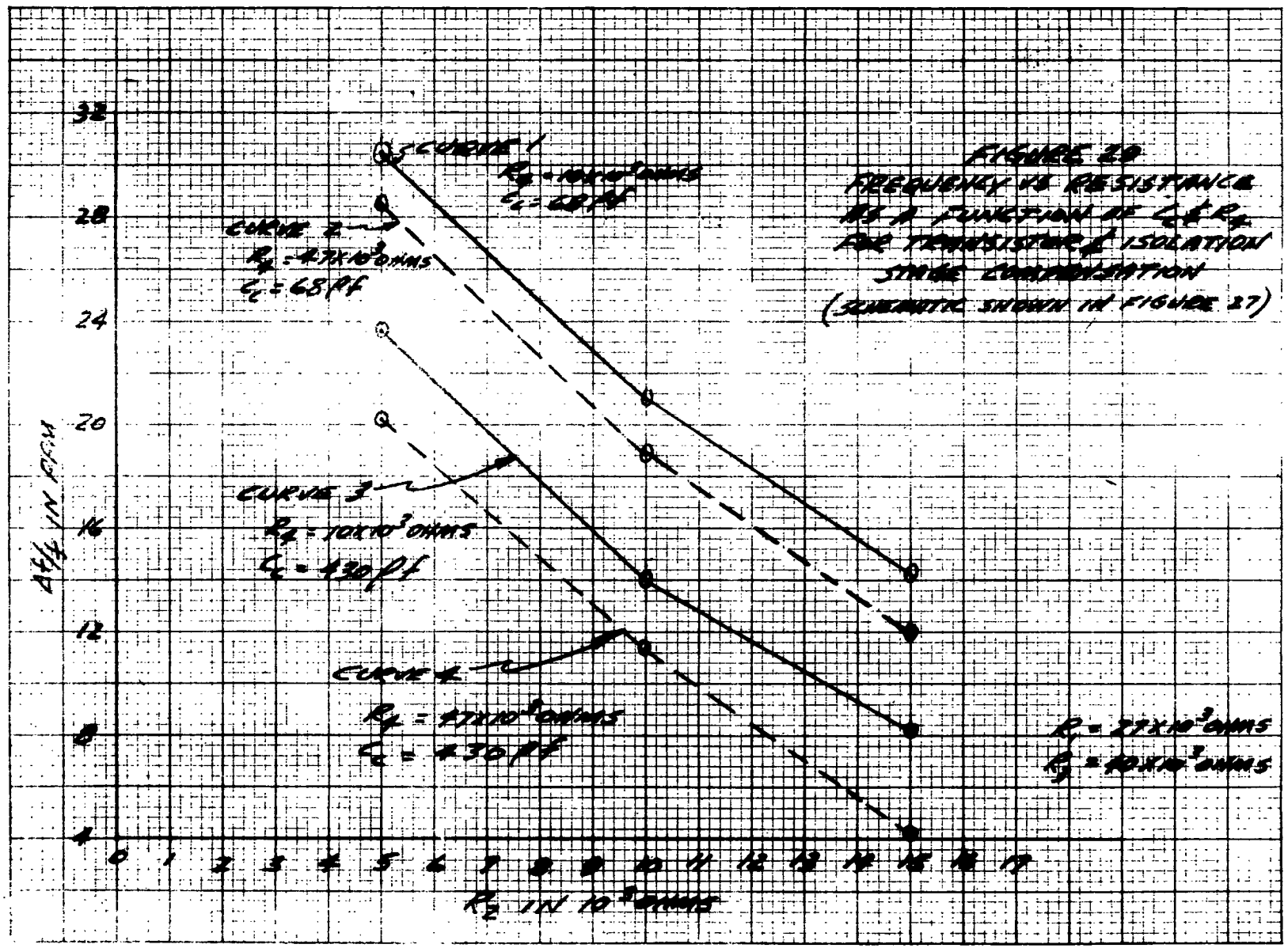


FIGURE 29
FREQUENCY VS RESISTANCE AS A FUNCTION OF C_c & R_2 FOR TRANSISTOR ISOLATION STAGE COMPENSATION (SCHEMATIC SHOWN IN FIGURE 27)

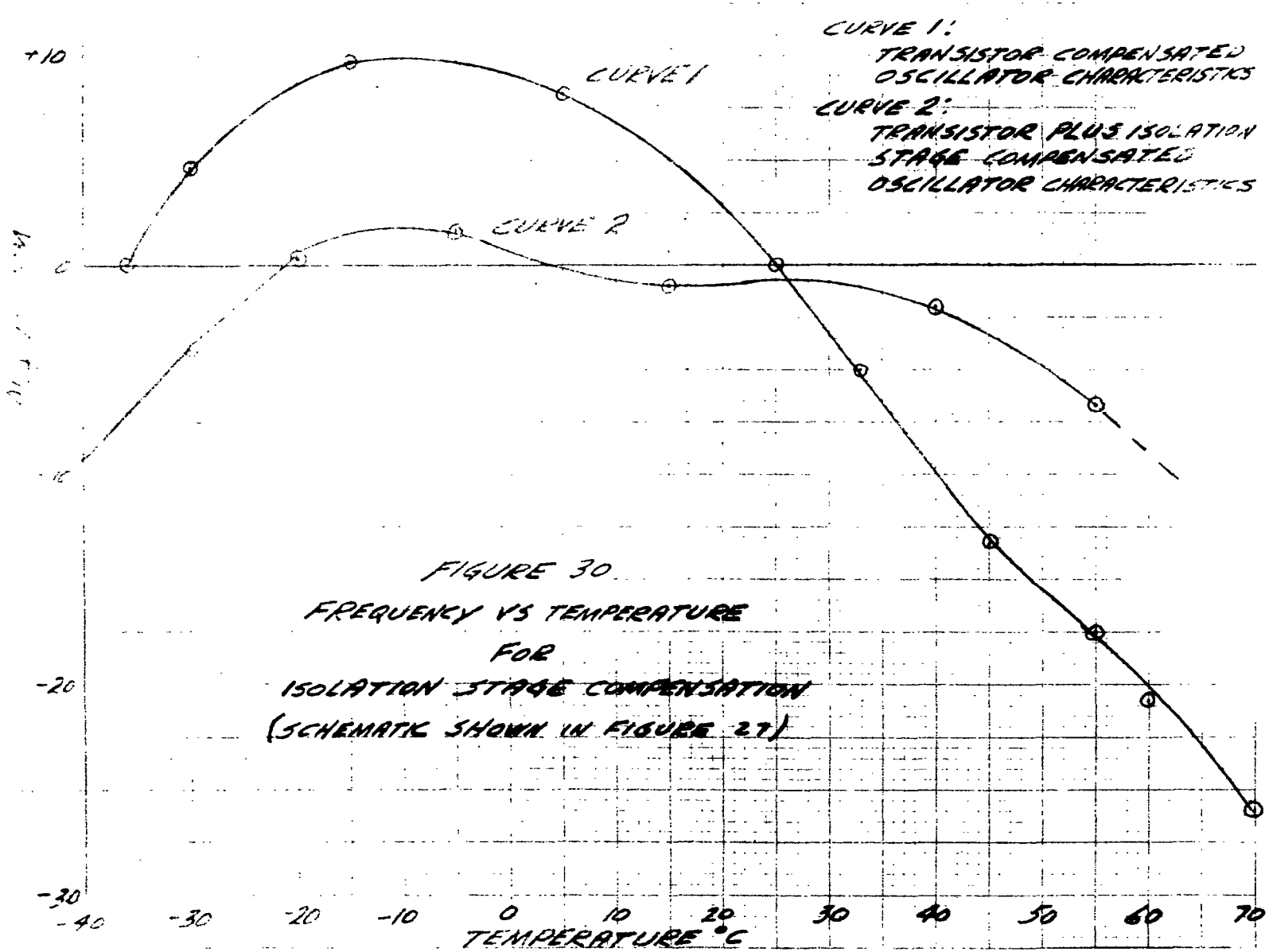


FIGURE 30

FREQUENCY VS TEMPERATURE

FOR

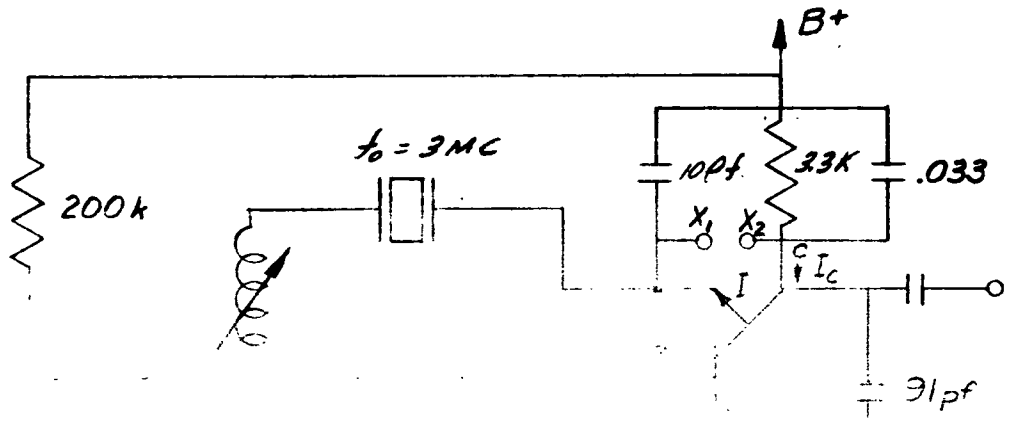
ISOLATION STAGE COMPENSATION

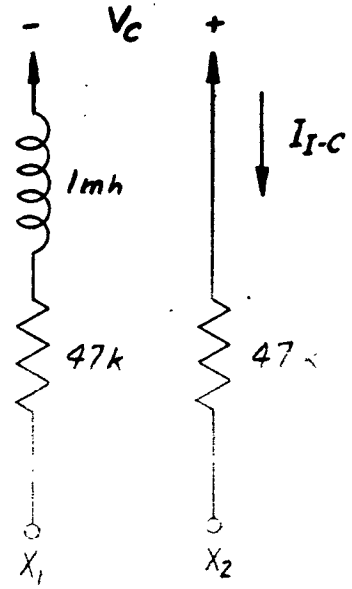
(SCHEMATIC SHOWN IN FIGURE 27)

4.6 Binistor Compensation Method

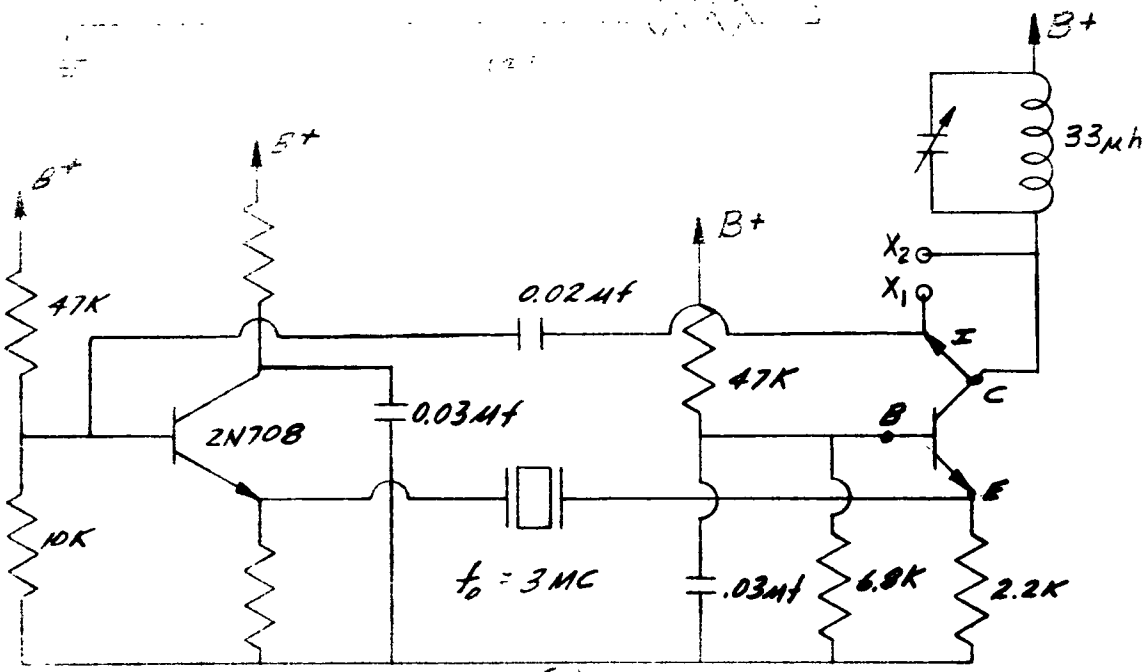
At the present time, the binistor method of compensation has not been investigated very thoroughly. A number of binistors have been tested to determine if they exhibit the required characteristics. The test oscillator configurations are shown in Figure 31. The results obtained are shown in Figure 32. The action of the binistor was not as predicted. The various currents in the circuit are shown plotted in Figure 33, as a function of V_{ci} (voltage from collector to injector). The current through the collector to injector junction was not anticipated. More binistors are now on order, so that a more thorough investigation of their characteristics can be made.

The capacitance across the collector to injector junction of the two binistors tested appears to be too small for practical use. This is due to the fact that this capacitance does not have any limiting manufacturing specifications. The possibility of obtaining either selected binistors with larger junction capacities or specially made binistors with larger injector to collector junction areas has been discussed with a representative from Transitron. The feasibility of obtaining a number of binistors on consignment for our immediate requirements was discussed, but no definite answer has been received.

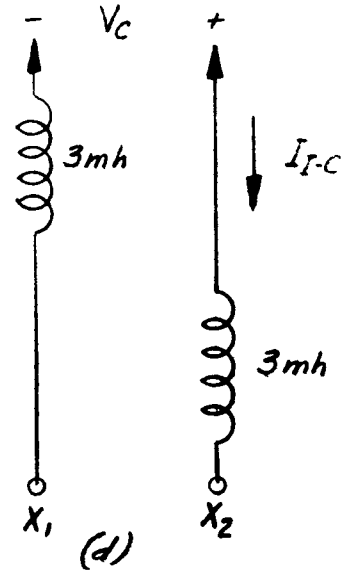




(b)



(c)



(d)

SCHEMATICS FOR SINISTOR COMPENSATED TEST OSCILLATORS
FIGURE 31

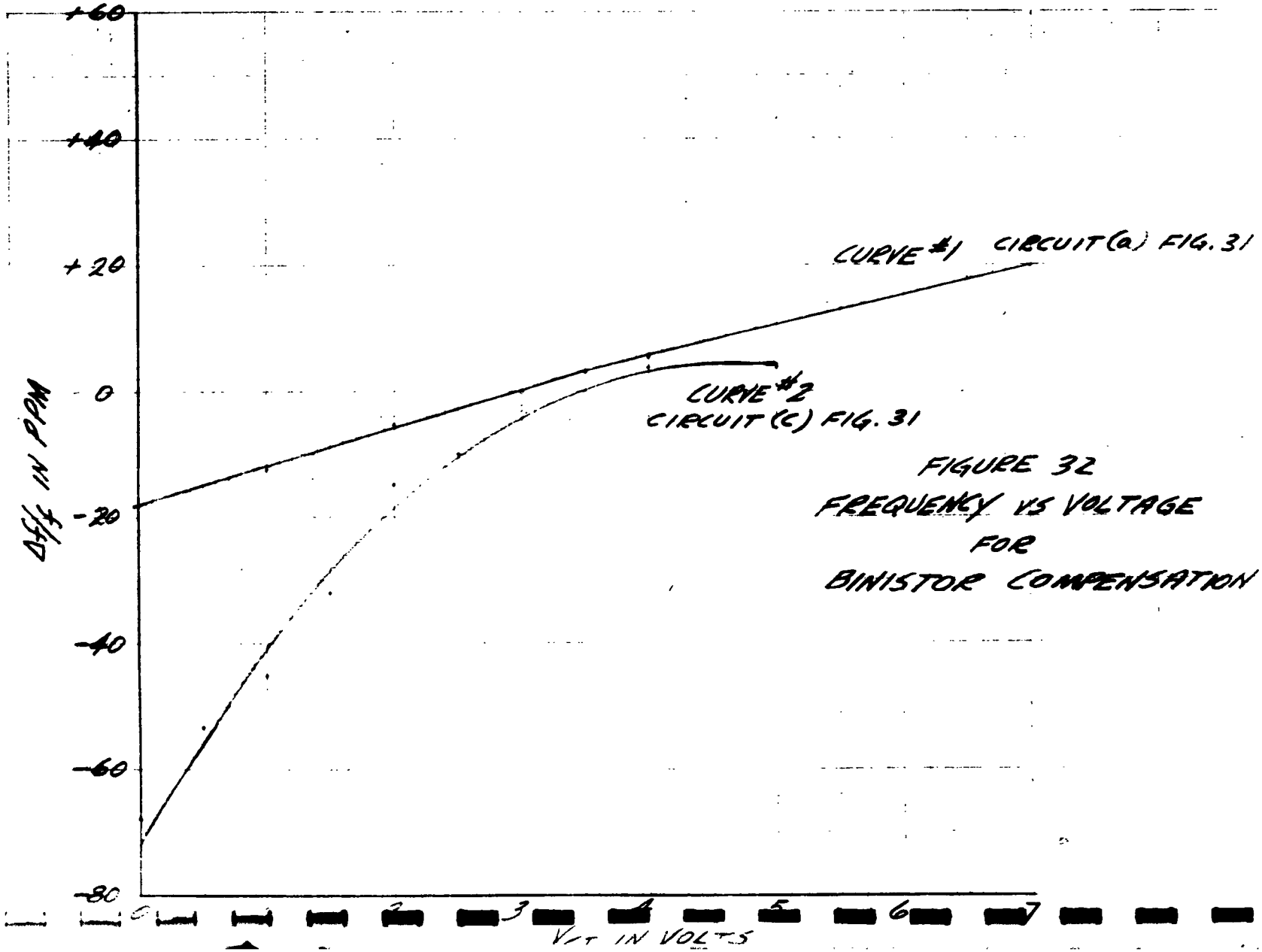


FIGURE 32
FREQUENCY VS VOLTAGE
FOR
BINISTOR COMPENSATION

SCHEMATIC FOR CURVE 1 SHOWN IN FIGURE 3(a)
SCHEMATIC FOR CURVE 2 SHOWN IN FIGURE 3(b)
SCHEMATIC FOR CURVE 3 SHOWN IN FIGURE 3(c)

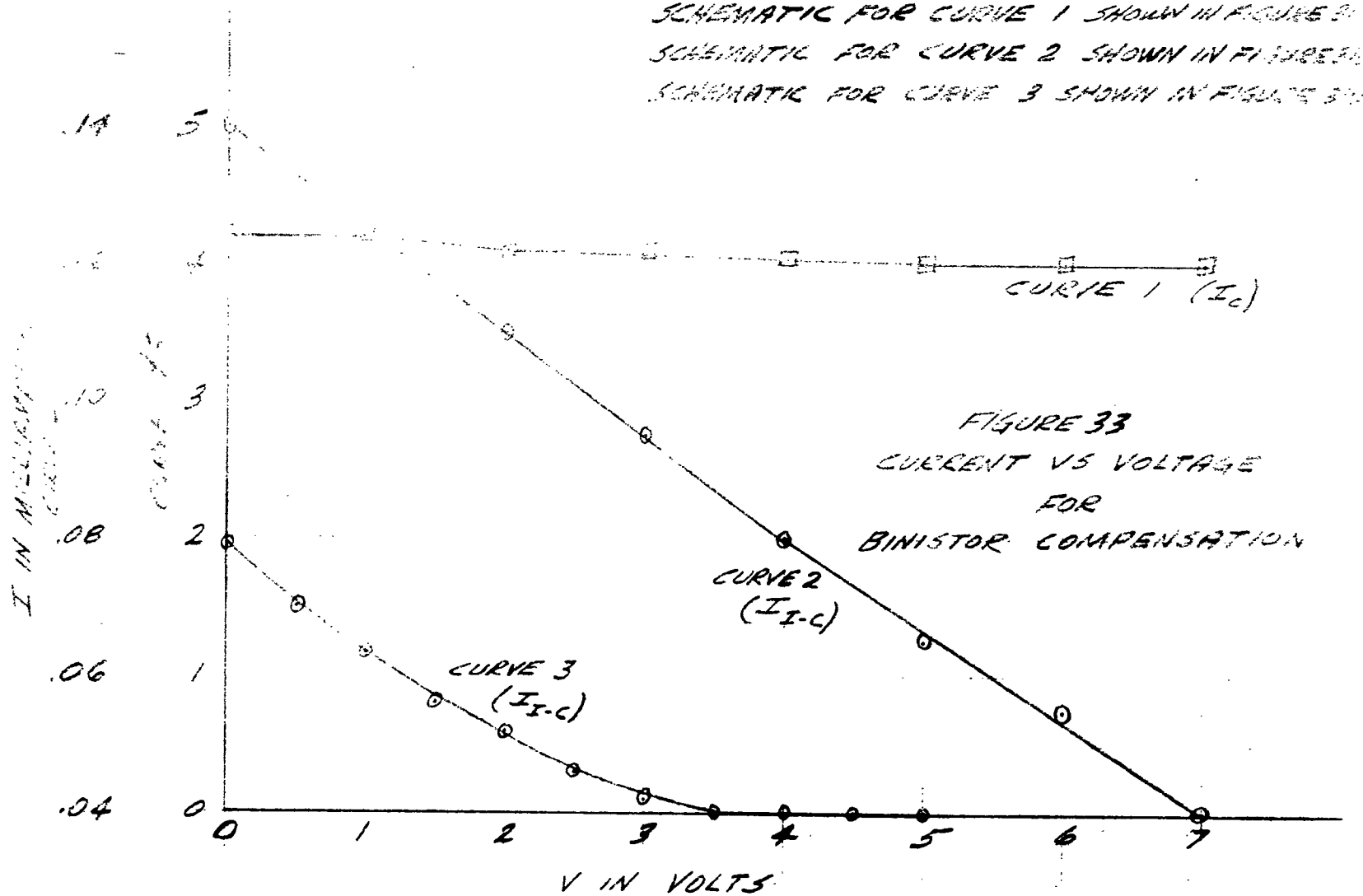


FIGURE 33
CURRENT VS VOLTAGE
FOR
BINISTOR COMPENSATION

4.7 Capacitor - Diode Method - Mathematical Analysis

The method of compensation discussed in this section of the report utilizes a semiconductor diode and a fixed capacitor, therefore, is referred to as the diode-capacitor method of compensation. The first time that this method was tried for compensation, the results were quite favorable and a thorough investigation was initiated. Figure 34a shows the basic oscillator schmatic utilizing the diode capacitor method of compensation. The diode D_1 is a silicon diode, biased in the forward direction and capacitor C_x is a fixed capacitor. At the points denoted by (X) the d-c control circuit is connected. The d-c control network is shown in Figure 34b. The combination of this network with D_1 and C_x forms the entire compensation circuit. In Figure 34b, R_c denotes coupling resistors, Z_1 and Z_2 are temperature sensitive resistance networks, and the voltage source E is constant. The a-c equivalent circuit of the compensation circuit is shown in Figure 35b. R_D represents the diode D_1 and control network in Figure 35a. Figure 36 is a plot of a typical voltage versus current curve for a silicon diode. As the current through the diode increases, the voltage also increases in a non-linear manner. R_D is the slope of the V-I curve at any point as shown on the curve at Point (a). It is apparent that as the d-c current through the diode increases the a-c resistance decreases. Figure 35c is the series a-c equivalent circuit of the parallel equivalent circuit in Figure 35b.

$$\text{(a)} \qquad R_s = \frac{R_p}{R_p^2 \omega^2 C_p^2 + 1}$$

$$\text{(b)} \qquad C_s = C_p \left(1 + \frac{1}{\omega^2 C_p^2 R_p^2}\right)$$

Equations (a) and (b) give the relationships between the series and parallel circuits in Figure 35. Assuming that ω is constant and C_p is constant, Figure 37 is a plot of normalized R_s and $1/\omega C_s$ versus R_p. As R_p varies from infinity to 0,

R_s varies from 0 to infinity. Also as R_p varies from infinity to 0, C_s varies from C_p to infinity at $|R_p| = \left|\frac{1}{\omega C_p}\right|$, R_s is equal to $R_p/2$ and $C_s = 2C_p$. Therefore, the resistance, R_s placed in series with the crystal will always be less than R_p and the series capacitance C_s will always be greater then C_p. If the fixed capacitance C_p and the V-I curve for the diode are known, then the plot of C_s versus I can be determined. This can then be used in further calculations for the required I versus temperature, and consequently the Z_1 and Z_2 versus temperature required for compensation.

The following analysis was done to give an indication of the effect of R_D upon the Q of the oscillator. Figure 38a is the equivalent oscillator circuit used in this analysis. L_1, C_1, R_1 and C_o are constants of the crystal, R_D and C_D are the compensating networks and R_y, C_y and -R are the equivalent parameters looking back into the oscillator from the crystal and compensation network terminal.

The following analysis is an attempt to find an order of magnitude effect of the diode-capacitor method of compensation on the Q of the oscillator.

$$(1) \qquad R_a = \frac{R_D}{R_D^{\,2}\,\omega^2 C_D^{\,2} + 1}$$

$$(2) \qquad C_a = C_D \left(1 + \frac{1}{\omega^2 C_D^{\,2}\, R_D^{\,2}}\right)$$

$$(3) \qquad R_b = \frac{R_y}{R_y^{\,2}\,\omega^2\, C_y^{\,2} + 1}$$

$$(4) \qquad C_b = C_y \left(1 + \frac{1}{\omega^2 C_y^{\,2}\, R_y^{\,2}}\right.$$

From equations (1) through (4), the circuit shown in Figure 38a can be reduced to the circuit in Figure 38b. The circuit in Figure 38b can be reduced still further to the one shown in Figure 38c by using equations (5) and (6).

(5) $R_m = R_a + R_b$

(6) $C_m = \dfrac{C_a \; C_b}{C_a + C_b}$

Now combining C_o with R_m and C_m, the following relationships result and are shown in Figure 38d.

(7) $$Z_T = \frac{\frac{R_m^2}{\omega^2 C_o^2} - j\frac{R_m^2}{\omega C_o} + \frac{1}{\omega^3 C_o^2 C_m} + \frac{1}{\omega^3 C_o C_m^2}}{R_m^2 + \frac{1}{\omega^2}\left(\frac{C_o + C_m}{C_o \; C_m}\right)}$$

(8) $$R_T = \frac{R_m}{\left(\frac{C_o}{C_m} + 1\right)^2 + R_m^2 \, \omega^2 C_o^2}$$

(9) $$C_T = \frac{R_m^2 \, C_o^2 \, C_m^2 + \frac{1}{\omega}(C_o + C_m)^2}{R_m^2 \, \omega C_o \, C_m^2 + \frac{C_m}{\omega} + \frac{C_o}{\omega}}$$

The circuit presented in Figure 38a has not been reduced to an equivalent series circuit as shown in Figure 38d. To continue our investigation to determine the effect of the diode compensation method on the Q of the circuit, assume the following parameters for circuit 38a.

$W = 20 \times 10^6$ cps

$C_D = 50 \times 10^{-12}$ f

$C_y = 50 \times 10^{-12}$ f

$R_y = 5 \times 10^3$ ohm

$C_o = 5 \times 10^{-12}$

R_D = unknown value

$$R_T = \frac{0.2 \times 10^3 + \frac{R_D}{R_D^2 \times 10^{-6} + 1}}{\left(\frac{100 \times 10^{-12} + \frac{5 \times 10^{-5}}{R_D^2}}{5 \times 10^{-10} + \frac{5.2 \times 10^{-4}}{R_D^2}} + 1\right)^2 + \left(0.2 \times 10^3 + \frac{R_D}{R_D^2 \times 10^{-6} + 1}\right)^2} \times 10^{-8}$$

If R_D = infinity

R_T = 139 Ω

R_D = 0

R_T = 167 Ω

If $R_D = R_D \left|\frac{1}{\omega C_D}\right|$, R_D is equal to 1000 Ω

then:

R_T = 900 Ω

The relationship for Q of the circuit in Figure 3(d) is given in Equation (10).

$$(10) \qquad Q = \frac{\omega L_1}{R_1 + R_T}$$

The ratio of circuit Q's with and without the compensation network is given by Equation (11).

$$(11) \qquad \frac{Q_o}{Q_x} = \frac{\left(\frac{\omega L_1}{R_1 + R_T}\right) R_D = 0}{\left(\frac{\omega L_1}{R_1 + R_T}\right) R_D = K} = \frac{(R_1 + R_T) \quad R_D = K}{(R_1 + R_T) \quad R_D = 0}$$

The maximum effect of R_D is when $R_D = \left|\frac{1}{\omega C_D}\right|$, therefore, the worst degradation of circuit Q will be when the following condition exists:

$$(12) \qquad \sigma = \left(\frac{Q_o}{Q_x}\right)_{MAX} = \frac{(R_1 + R_T) \quad R_1 = \left|\frac{1}{\omega C_D}\right|}{(R_1 + R_T) \quad R_1 = 0}$$

Therefore in this example:

$$(13) \qquad \sigma = \frac{R_1 + 900}{R_1 + 167}$$

The very maximum value for σ that could be obtained is when $R_1 = 0$. In this case, σ = 900/167 = 5.4. If R_1 is kept above or below the value $\left|\frac{1}{\omega C_D}\right|$ then σ will decrease correspondingly.

The value for R_T without compensation can be checked to see if it is of the right order of magnitude by considering the following equations.

If:

(14) $$Q_o = \frac{\omega L_1}{R_1 + R_T}$$

then:

(15) $$R_T = \frac{\omega L_1 - R_1 Q_o}{Q_o} = \frac{\omega L_1}{Q_o} - R_1$$

If it is further assumed that $C_o/C_1 = 300$, then:

(16) $$L_1 = .15 \text{ HENRIES}$$

therefore:

(17) $$R_T = \frac{3 \times 10^6}{Q_o} - R_1$$

The following table gives values of R_T for various assumed values of Q_o and R_1.

R_T - Ω	Q_o	R_1 - Ω
300×10^3	10	10
30×10^3	100	10
2.990×10^3	1000	10
290 Ω	10000	10
299.9×10^3	10	100
29.9×10^3	100	100
2.9×10^3	1000	100
200 Ω	10000	100

From the table above it appears as if R_T is too low and, consequently, the assumed values for R_y and C_y in Figure 38a were probably too low. By obtaining more accurate values for the circuit parameters a more realistic value for R_T would probably be obtained. If R_T is larger in magnitude than was indicated in the example given, then the maximum ratio between $(Q_o)\ R_D = K/\ (Q_o)\ R_D = 0$ would be less, indicating that the effect of the diode resistance would have very little effect on the Q of the oscillator.

The temperature dependent resistance network in Figure 35a acts as a current generator for diode D_1 and it represents an open circuit to a-c signals. This is true in actual compensation circuitry because R_c is very large. Therefore, the diode characteristics do not affect the diode current. The relationships of I_D to the rest of the circuit parameters is derived in the following analysis.

Consider the circuit in Figure 35a.

(18) $$E = I_1 (Z_1 + Z_2) - I_D (Z_2)$$

(19) $$0 = -I_1 (Z_2) + I_D (Z_2 + 2 R_c + R_n)$$

(20) $$I_o = \frac{I_1 (Z_2)}{Z_2 + 2 R_c + R_n}$$

(21) $$E = I_o \left(\frac{Z_2 + 2 R_c + R_n}{Z_2}\right)(Z_1 + Z_2) - I_D (Z_2)$$

(22) $$E = I_o \left(1 + \frac{2R_c}{Z_2} + \frac{R_n}{Z_2}\right) \left(Z_1 + Z_2\right) - Z_2$$

(23) $$I_o = E \Big/ \left(1 + \frac{2R_c}{Z_2} + \frac{R_n}{Z_2}\right) \left(Z_1 + Z_2\right) - Z_2$$

(24) $$R_c >> R_n = E \Big/ \left(1 + \frac{2R_c}{Z_2}\right) \quad (Z_1 + Z_2) - Z_2$$

(25) $$I_o = E \Big/ Z_1 + Z_2 + 2R_c \left(1 + \frac{Z_1}{Z_2}\right) = E \Big/ Z_1 + 2R_c \left(1 + \frac{Z_1}{Z_2}\right)$$

If $R_c >> Z_1$, then:

(26) $$I_o = E \Big/ 2R_c \left(1 + \frac{Z_1}{Z_2}\right) = Z_2 \; E \Big/ 2R_c \quad (Z_1 + Z_2) \approx V_o \Big/ 2R_c$$

I_o is approximately equal to the voltage divider's output voltage, V_o, divided by $2R_c$. As Z_2 becomes larger this relationship becomes less accurate and the exact equation must be used. I_o defines the resistance, R_D, of any given diode. Therefore, R_o can be determined easily if the diode V-I characteristics are known.

An analytical analysis of an oscillator using the capacitor-diode method of compensation can be made quite easily if the assumption is made that the resistance R_D is negligible. This assumption may or may not be true, depending on the exact component parameters used, but it simplifies calculations and gives an order of magnitude of the compensation network.

Assuming a circuit as shown in Figure 1, the following relationship must be known to arrive at an analytical analysis of the oscillator. Essentially, the analysis is the same as that for the varicap method, with the exception that a current source provides the compensation in the capacitance-diode method whereas a voltage source is used in the varicap method.

$$(1)\quad \frac{\Delta f}{f} = - m + \frac{2C_o \times 10^{-6}}{r\,(C_o + C_x)}$$

$$(2)\quad C_2 = f\,(R_D, C_D)$$

$$(3)\quad C_x = \frac{C_2 C_c}{C_2 + C_c}$$

T = TEMPERATURE

$$(4)\quad \frac{\Delta f}{f} = f\,(T)$$

$$(5)\quad R_D = f\,(I_D, T)$$

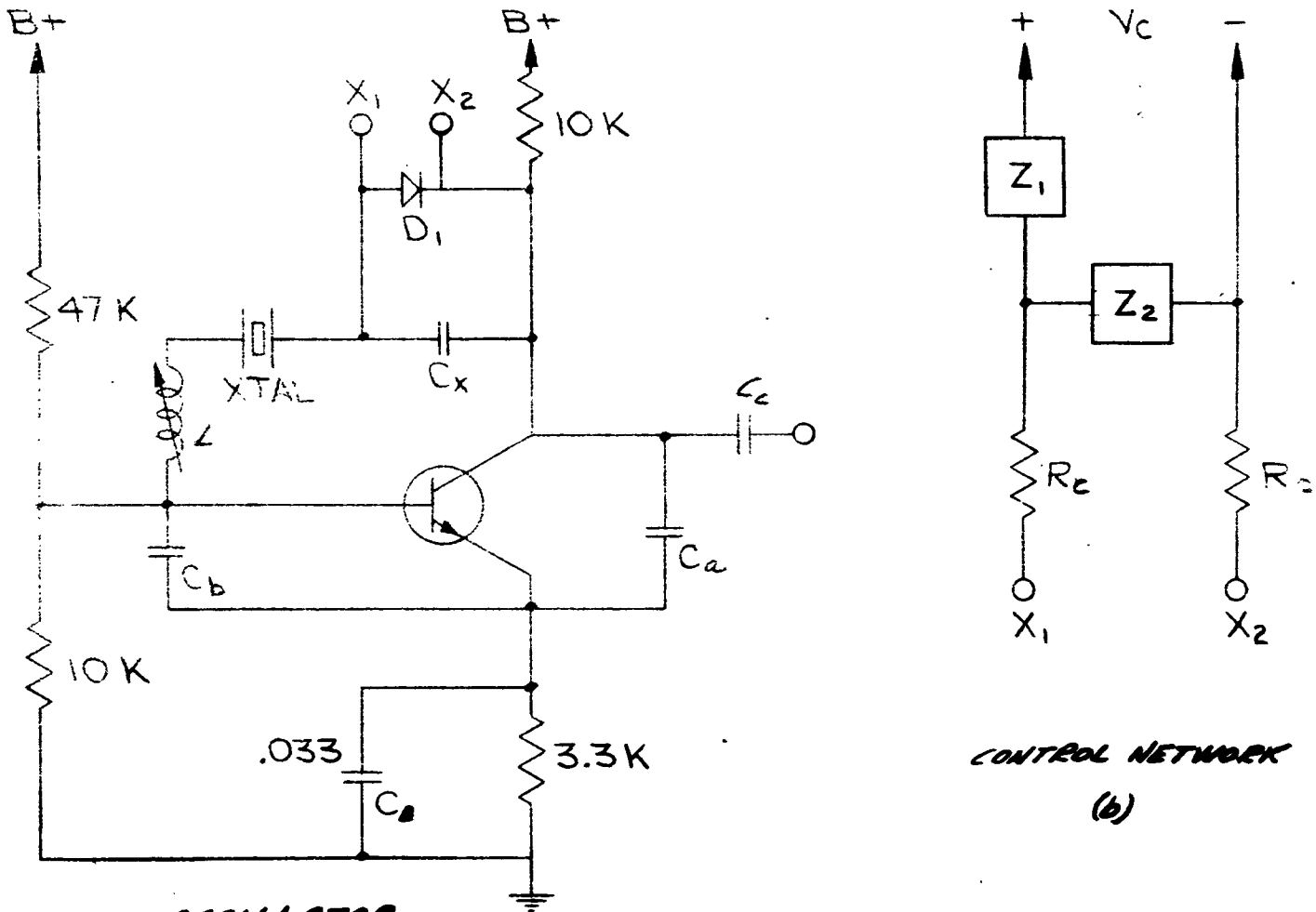
$$(6)\quad I_D = \frac{E\,Z_2}{Z_1\,(Z_2) + 2R_c\,(Z_1 + Z_2)} \qquad \frac{V_o}{2R_c}$$

$$(7)\quad Z_1 = f\,(T)$$

$$(8)\quad Z_2 = f\,(T)$$

In an analysis of this circuit, the variation of R_D with I_o and temperature must be known, the variation of P with C_x must be known, and C_c must be known.

With C_c known, the required value of C_s can be determined. From C_s and a given C_D, the required R_D as a function of temperature can be determined. From R_D the required I_o can be found and from I_o the required V_o, Z_1 and Z_2 can be found if E is known.



CAPACITOR-DIODE COMPENSATION CIRCUIT

FIGURE 34

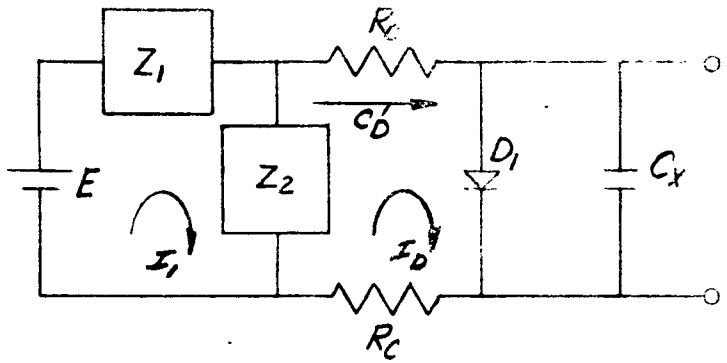


FIGURE 35 (a)

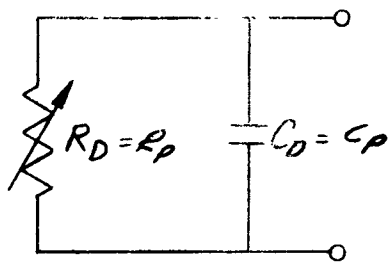


FIGURE 35 (b)

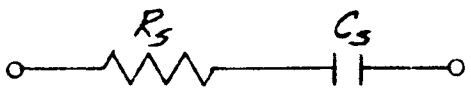


FIGURE 35 (c)

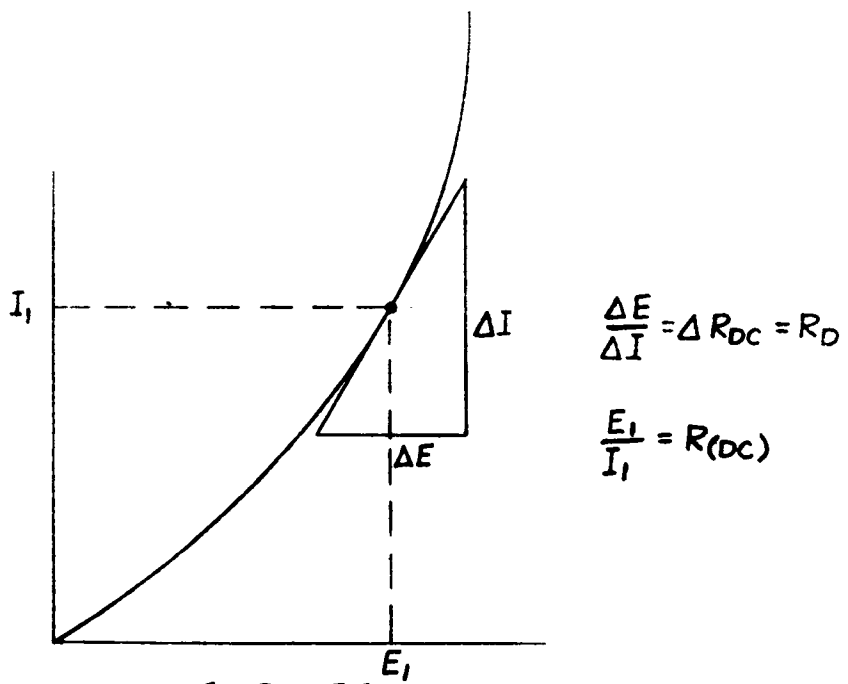


FIGURE 36

FIGURE 35 — CAPACITOR-DIODE COMPENSATION NETWORKS

FIGURE 36 — VOLTAGE-CURRENT CURVE FOR A SEMICONDUCTOR DIODE

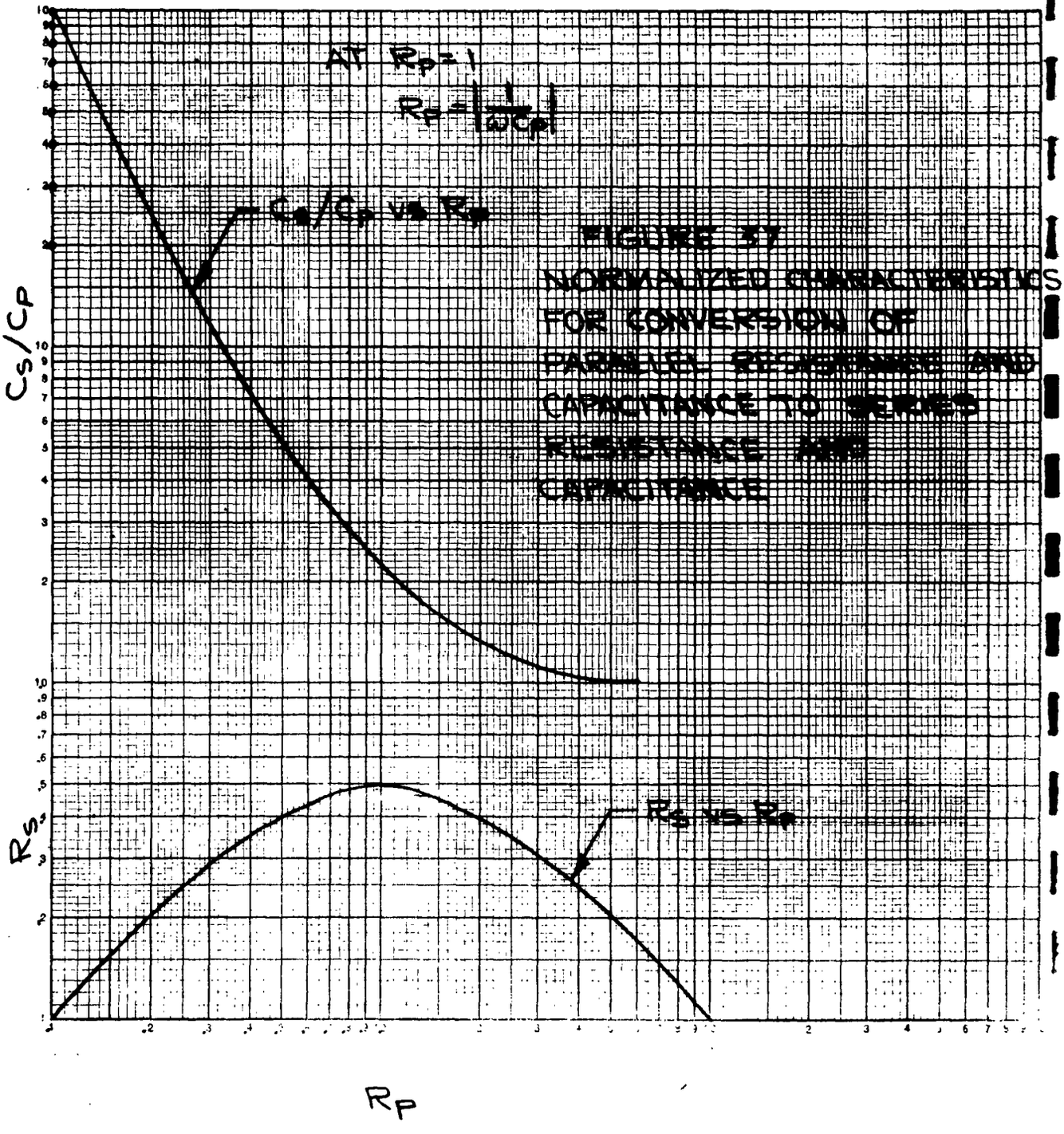
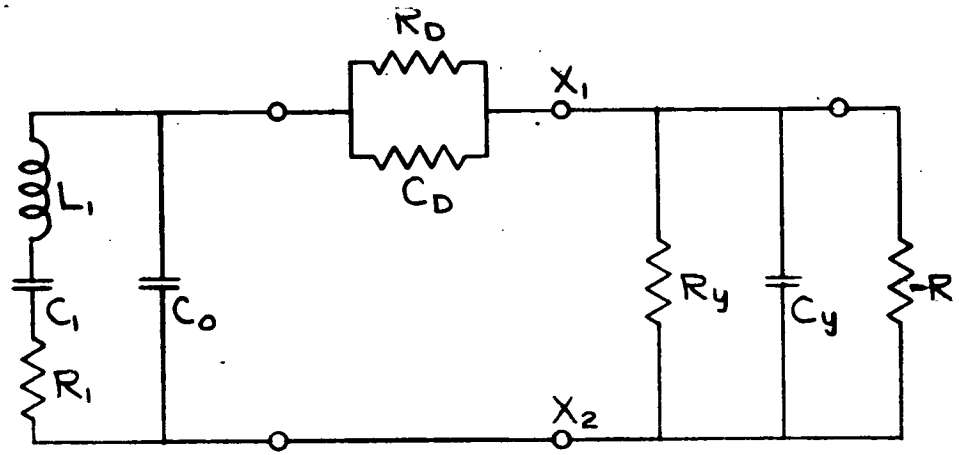
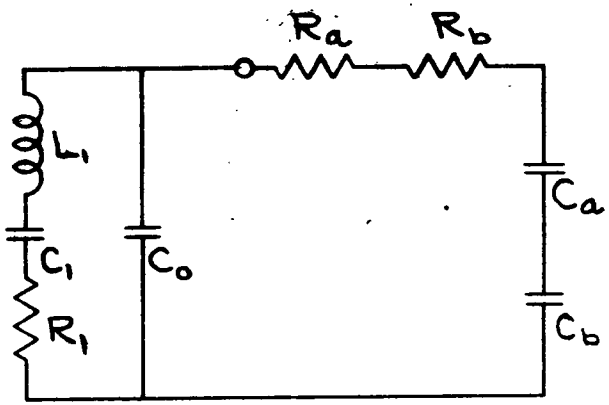


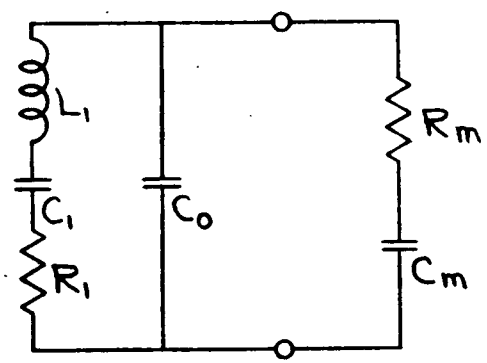
FIGURE 37
NORMALIZED CHARACTERISTICS FOR CONVERSION OF PARALLEL RESISTANCE AND CAPACITANCE TO SERIES RESISTANCE AND CAPACITANCE



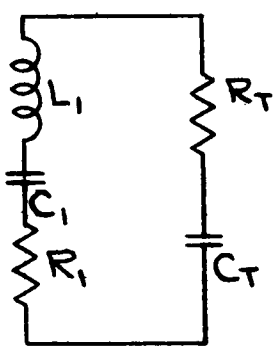
(a)



(b)



(c)



(d)

CIRCUITS FOR MATHEMATICAL ANALYSIS OF CRYSTAL-DIODE METHOD

FIG. 38

4.8 Capacitor - Diode Method: Empirical Analysis

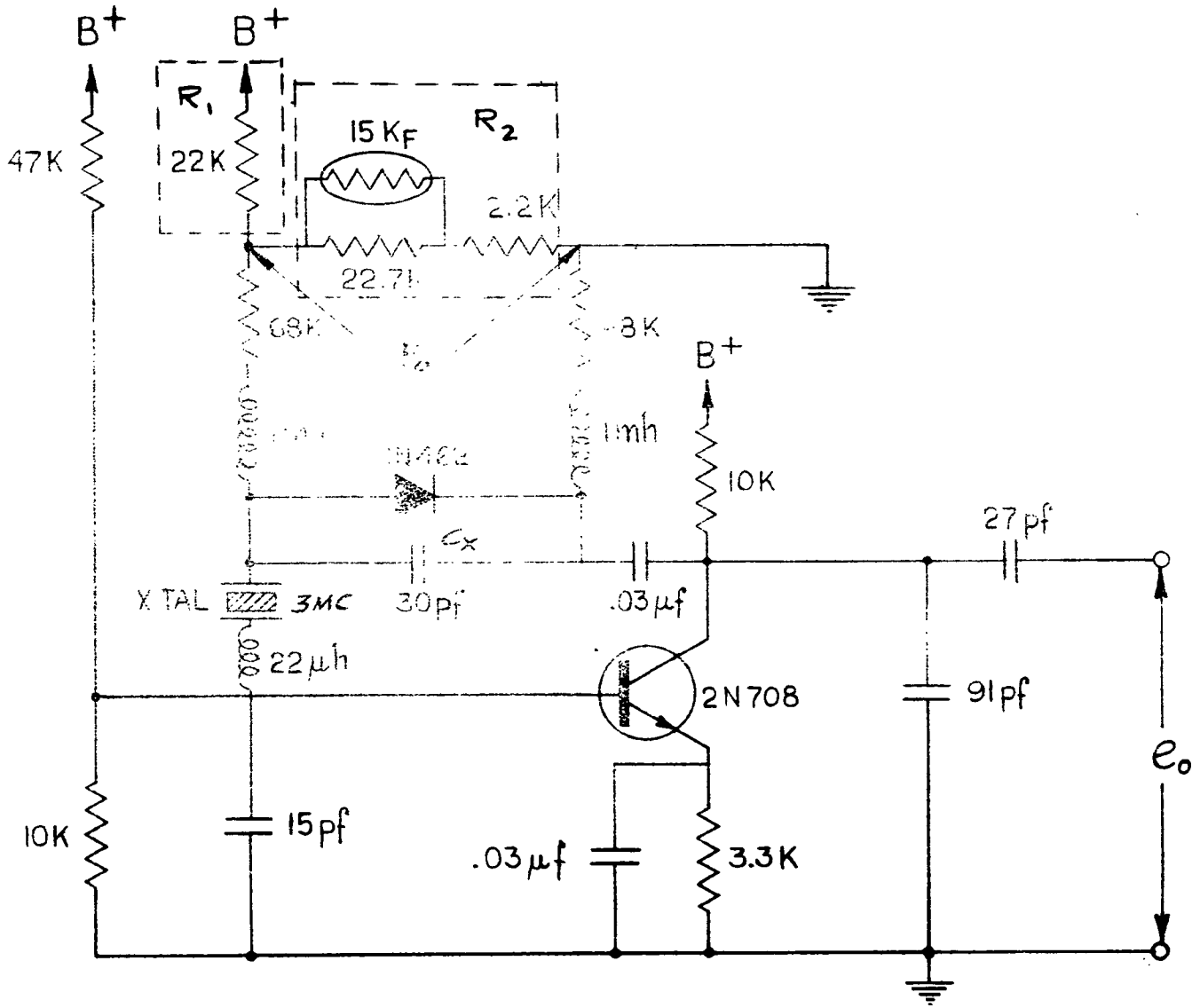
Using the basic principle presented in the preceding section, a number of oscillators were constructed and experimental data was obtained for the capacitor-diode method of compensation. Figure 39 is a schematic of the first oscillator built utilizing this method of compensation. Tests were conducted on the P versus V characteristics as a function of C_x as shown in Figure 40. The effect of changing C_x is apparent from the difference of the slope of the pullability curves in Figure 40. Thus varying C_x is an effective method of varying the pullability of the compensation network.

Tests following this initial circuit were performed on complete compensation circuits as shown in Figure 34. Curves of P versus R for various oscillators are shown in Figures 41, 42 and 43. The effect of temperature on the compensation network is also included in Graphs 41 and 42. The temperature effects on these curves is due to changes in the diode characteristics V versus I curve with temperature. This results in a change of R_D with temperature, and consequently, a change in frequency for a given diode current. The reason why some diodes are affected by temperature more than others is now being investigated to determine which diodes have the least temperature coefficient. To nullify the temperature coefficient of the diodes, C_x can be a negative temperature coefficient capacitor of the appropriate slope.

Figure 44 shows the P versus temperature curves of a capacitor-diode compensated oscillator. Curve #1 is the first try and curve #2 is the second try. This curve indicates the relative ease with which compensation can be obtained. The network for curve #1 is given in Figure 39. Curve #2 was obtained by putting a thermistor in the B+ leg of the divider. These networks were obtained from the set of curves shown in Figure 41. The method used to determine the appropriate networks was to examine the curves in Figure 41 and pick a suitable bias point for R_2. The R versus temperature function required to produce a compensating P versus temperature characteristics was then solved for in terms of actual network elements, thermistors and resistors. To compensate for the low end, it was assumed that P versus R_1 had the slope as P versus R_2 for values around R_2 = 22K. This is not exactly true, but is an approximate solution

Figure 45 shows the difference between a calculated compensation and the actual compensated oscillator frequency curve. The calculated and actual curve were in very good agreement considering the fact that temperature effects on the diode were not considered in the calculations.

Figures 46, 47 and 48 are plots of the best compensation curves obtained to this time, and the evolution of curve #4 from the original crystal curve is shown. The circuit used for these curves was similar to the one in Figure 39, except the 1 mh chokes were eliminated and the 68K resistors were increased to 82K.



DIODE - CAPACITOR COMPENSATION CIRCUIT FOR NETWORK NO. 3

FIGURE 39

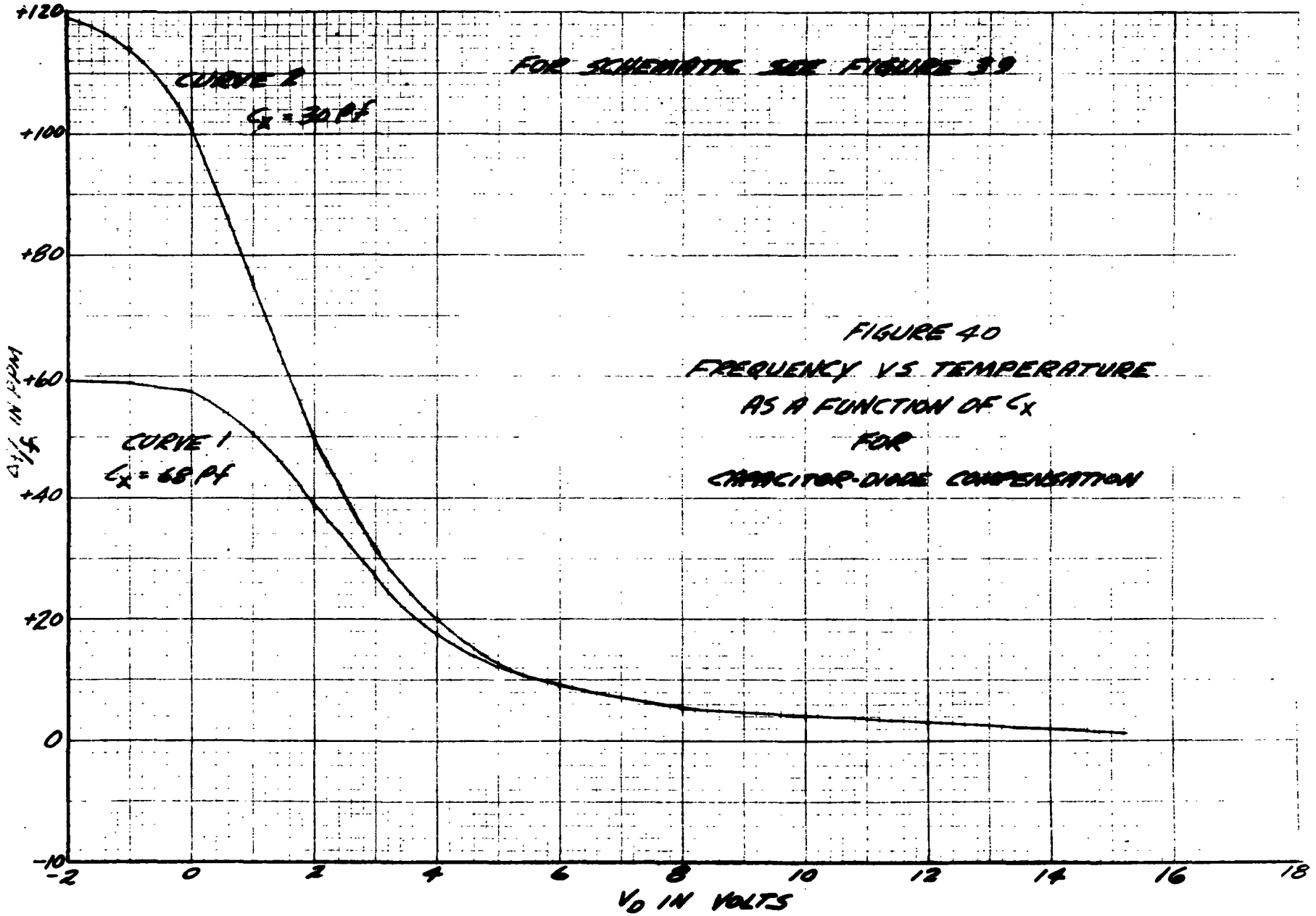


FIGURE 40
FREQUENCY VS TEMPERATURE
AS A FUNCTION OF C_x
FOR
CAPACITOR-DIODE COMPENSATION

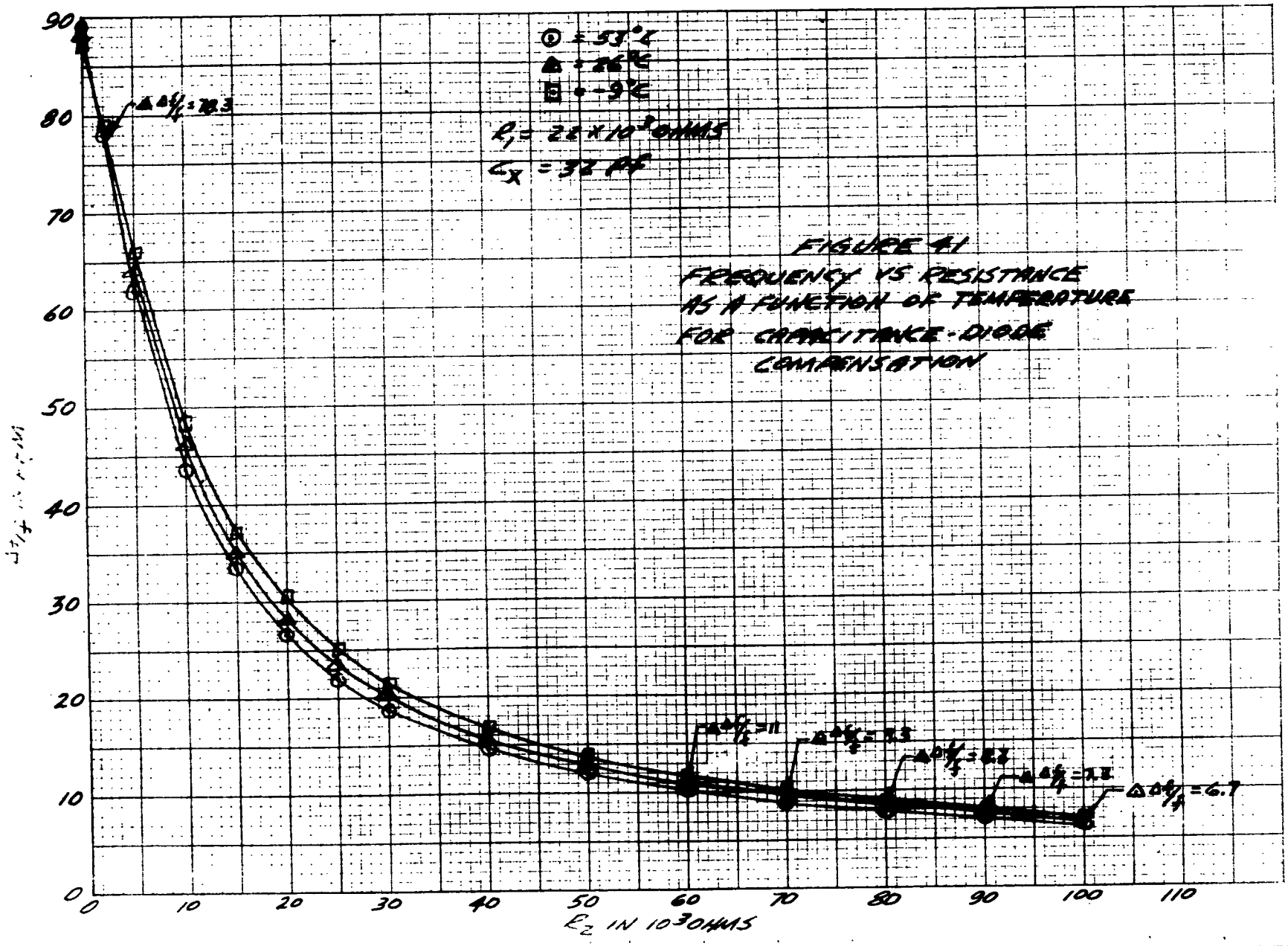
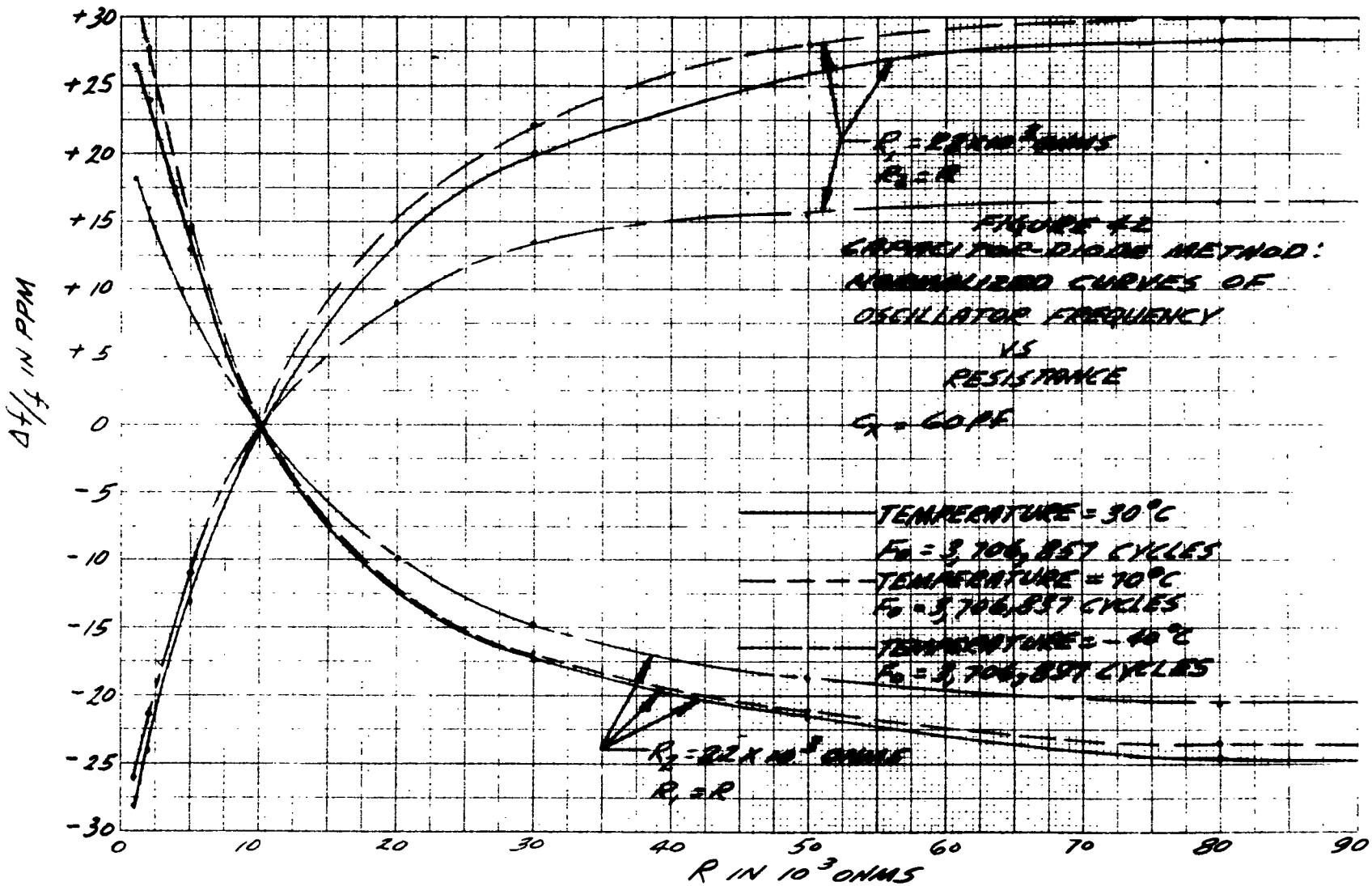


FIGURE 41
FREQUENCY VS RESISTANCE
AS A FUNCTION OF TEMPERATURE
FOR CAPACITANCE-DIODE
COMPENSATION


+30
+25
+20
+15
+10
+5
0
-5
-10
-15
-20
-25
-30
0
10
20
30
40
50
60
70
80
90
Δf/f IN PPM
R IN 10³ OHMS
FIGURE #2
CAPACITOR-DIODE METHOD:
NORMALIZED CURVES OF
OSCILLATOR FREQUENCY
VS
RESISTANCE
C_X = 60 PF
TEMPERATURE = 30°C
F_o = 3,706,857 CYCLES
TEMPERATURE = 70°C
F_o = 3,706,857 CYCLES
TEMPERATURE = -40°C
F_o = 3,706,857 CYCLES

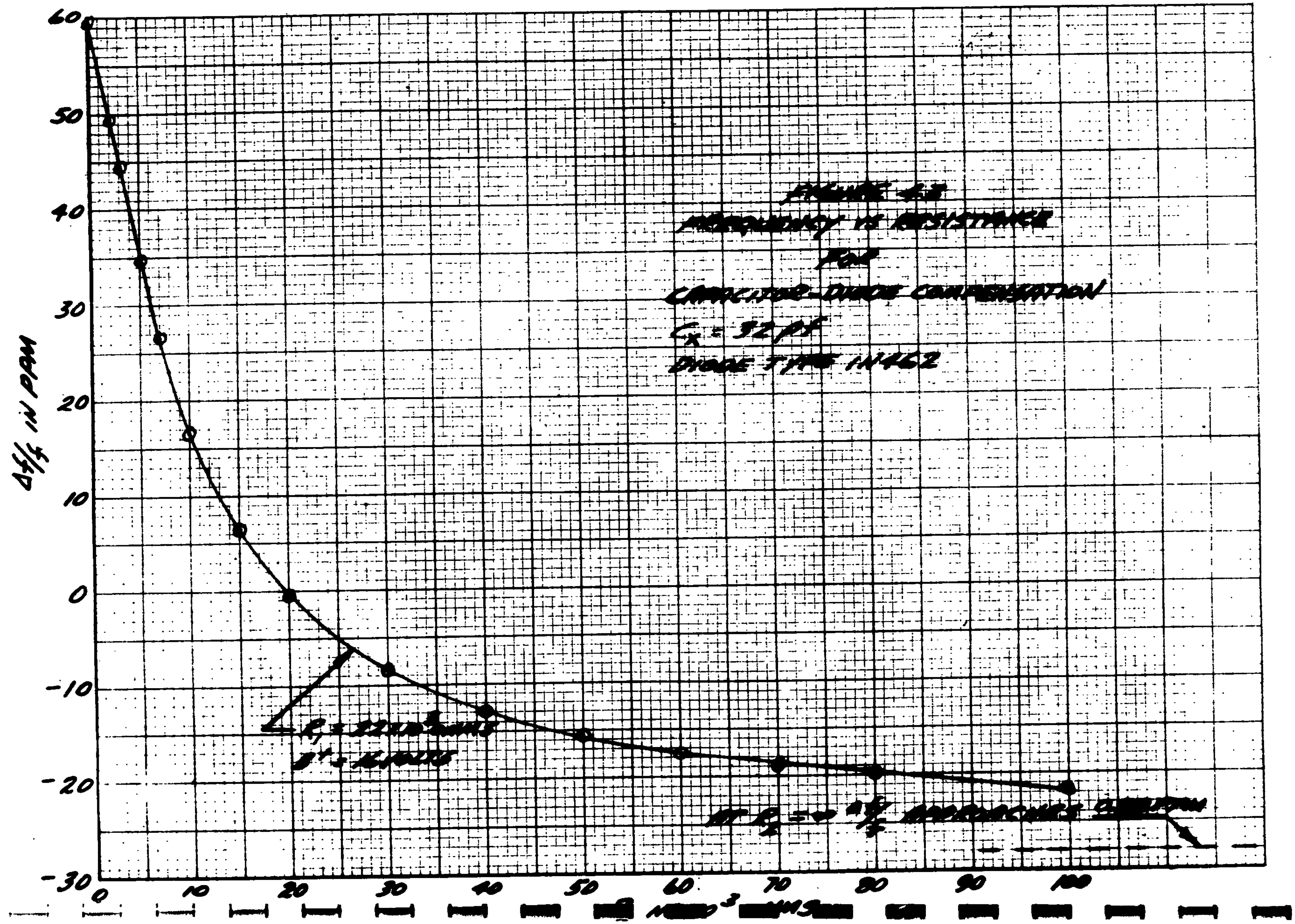


FIGURE 4.3
FREQUENCY VS RESISTANCE
FOR
CAPACITOR-DIODE COMPENSATION
C_X = 32 pf
DIODE TYPE 1N462
Δf/f IN PPM
60
50
40
30
20
10
0
-10
-20
-30
0
10
20
30
40
50
60
70
80
90
100

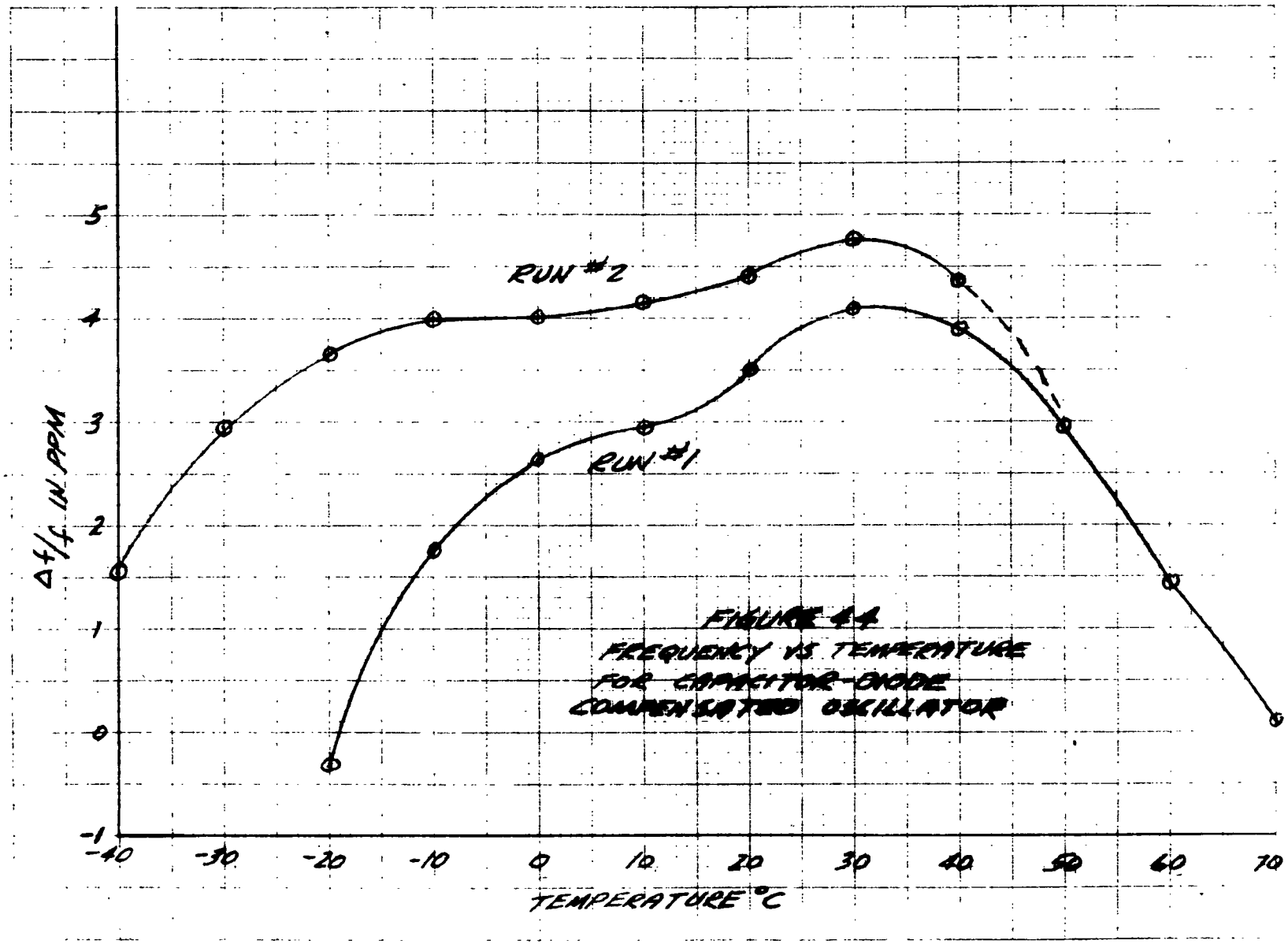


FIGURE 44
FREQUENCY VS TEMPERATURE
FOR CAPACITOR-DIODE
COMPENSATED OSCILLATOR

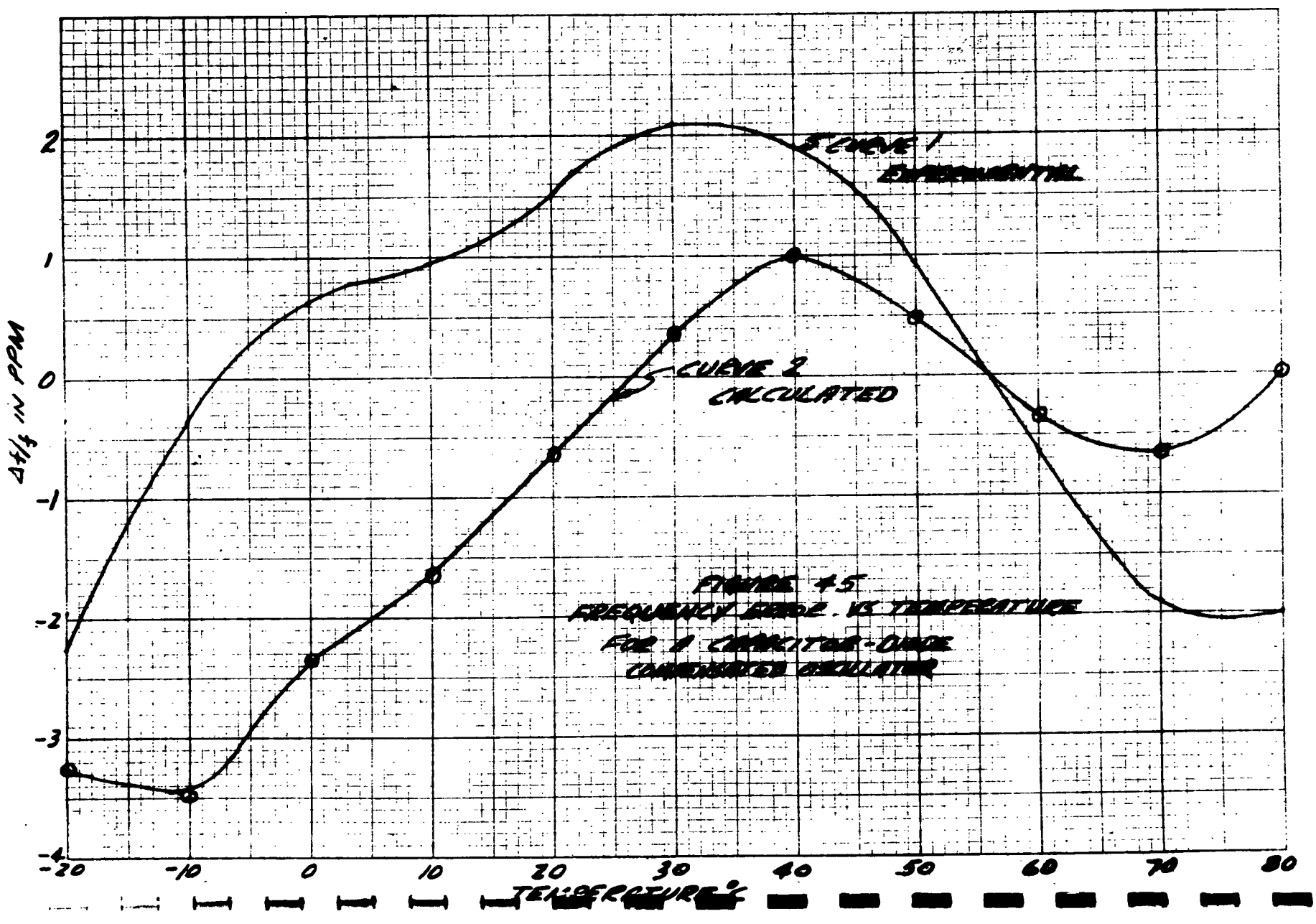
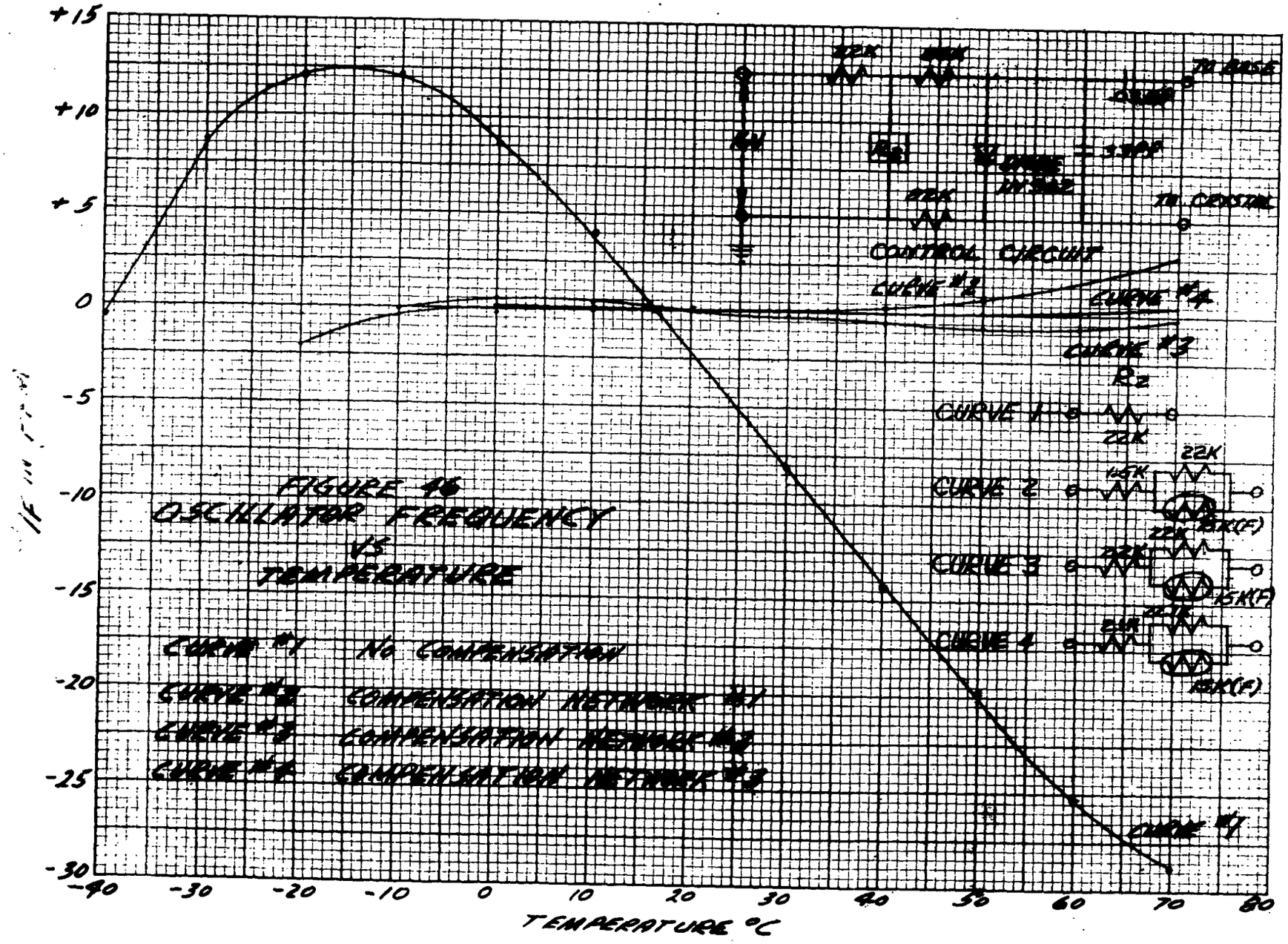


FIGURE 45
FREQUENCY ERROR IN TEMPERATURE
FOR A CRYSTAL-CONTROLLED
CONDENSER CIRCUIT


+15
+10
+5
0
-5
-10
-15
-20
-25
-30
-40
-30
-20
-10
0
10
20
30
40
50
60
70
80
TEMPERATURE °C
IF IN KC
FIGURE 16
OSCILLATOR FREQUENCY
VS
TEMPERATURE
CURVE #1 NO COMPENSATION
CURVE #2 COMPENSATION NETWORK #1
CURVE #3 COMPENSATION NETWORK #2
CURVE #4 COMPENSATION NETWORK #3
CONTROL CIRCUIT
CURVE #2
CURVE #4
CURVE #3
CURVE #1
CURVE 1
CURVE 2
CURVE 3
CURVE 4
22K
15K(F)

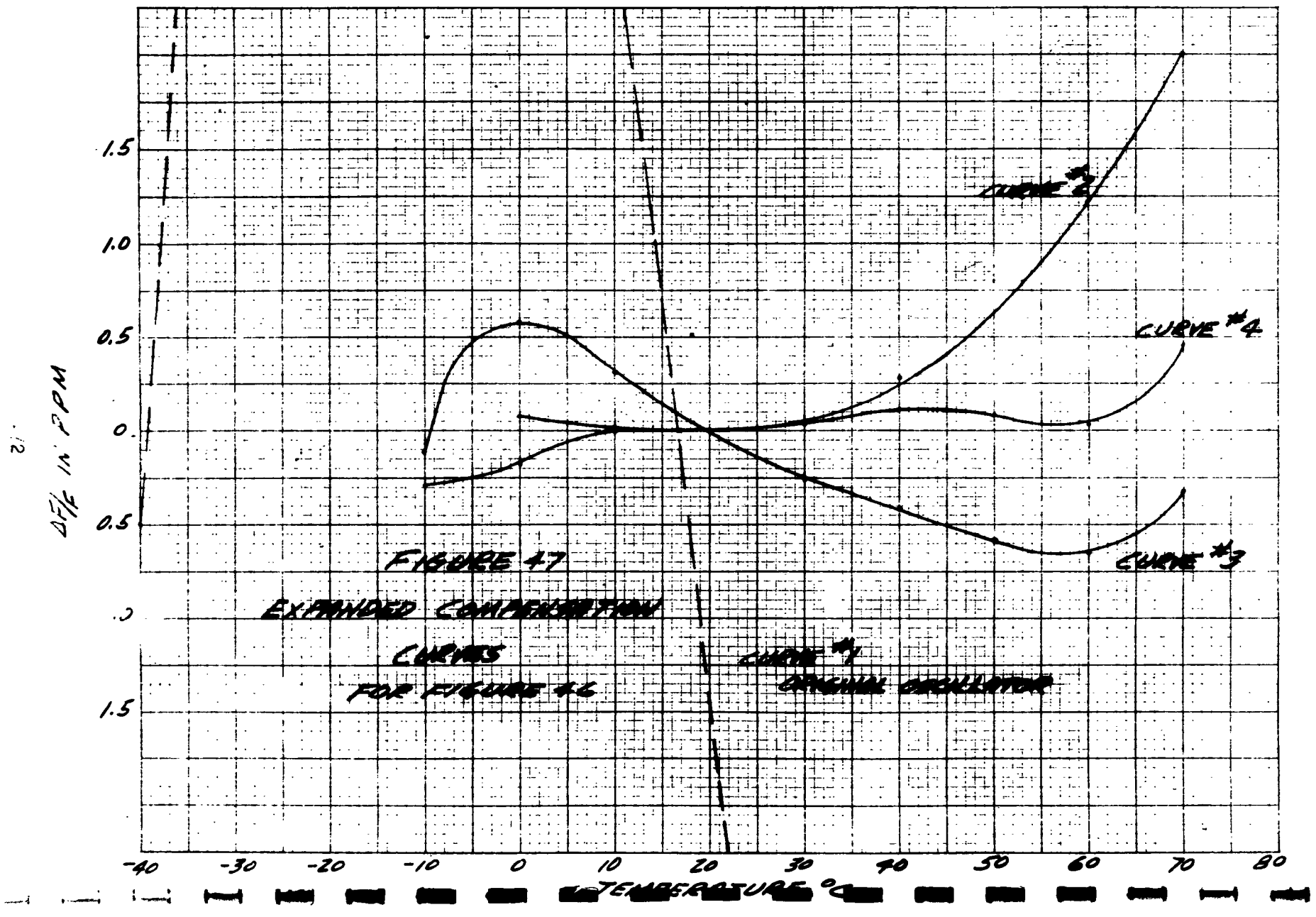


FIGURE 47

EXPANDED COMPENSATION CURVES FOR FIGURE #6

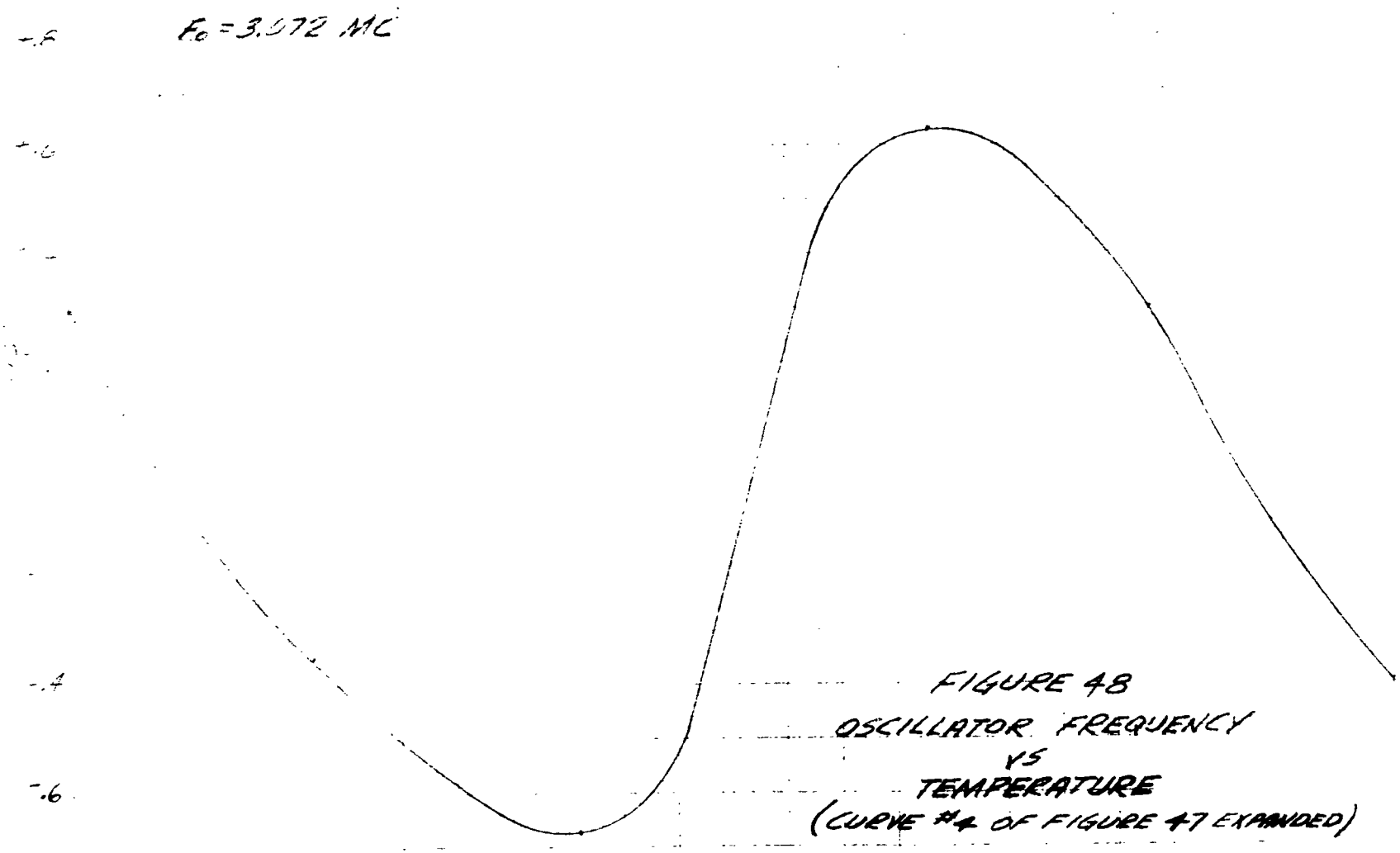


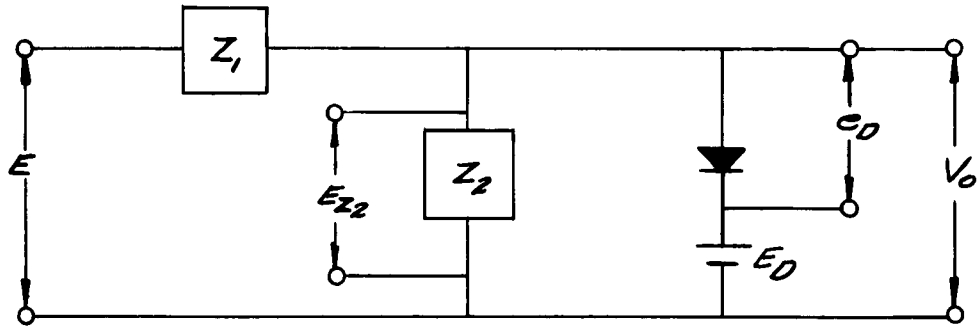
FIGURE 48
OSCILLATOR FREQUENCY
VS
TEMPERATURE
(CURVE #4 OF FIGURE 47 EXPANDED)

4.9 Diode voltage Control and Switching

The problem of generating specific voltage or resistance versus temperature curves has been discussed in the sections of this report on the various methods of compensation. The problem is essentially one of making a thermistor or thermistor network ineffective over a given temperature range and effective over the remaining temperature rnage. The first attempt at solving this problem is referred to as Diode Method a. This method uses semiconductor diodes to generate non-linear resistance and voltage curves with respect to temperature.

Method a:

The basic circuit for this method is shown schematically in Figure 49, where a diode is used to generate a non-linear voltage with respect to resistance.



DIODE CONTROLLED VOLTAGE DIVIDER
Figure 49

In the above circuit, Diode D_1 changes the normal output voltage, V_o, when D_1 is forward biased or $E_{Z2} \geq e_D + E_D$. As long as E_D is greater than E_{Z2}, D_1 is reverse biased and has an impedance much greater than Z_2. Therefore, D_1 is essential an open circuit.

E = supply voltage

Z_1 = thermistor network

Z_2 = thermistor network

D_1 = diode

E_D = bias voltage

V_o = output voltage

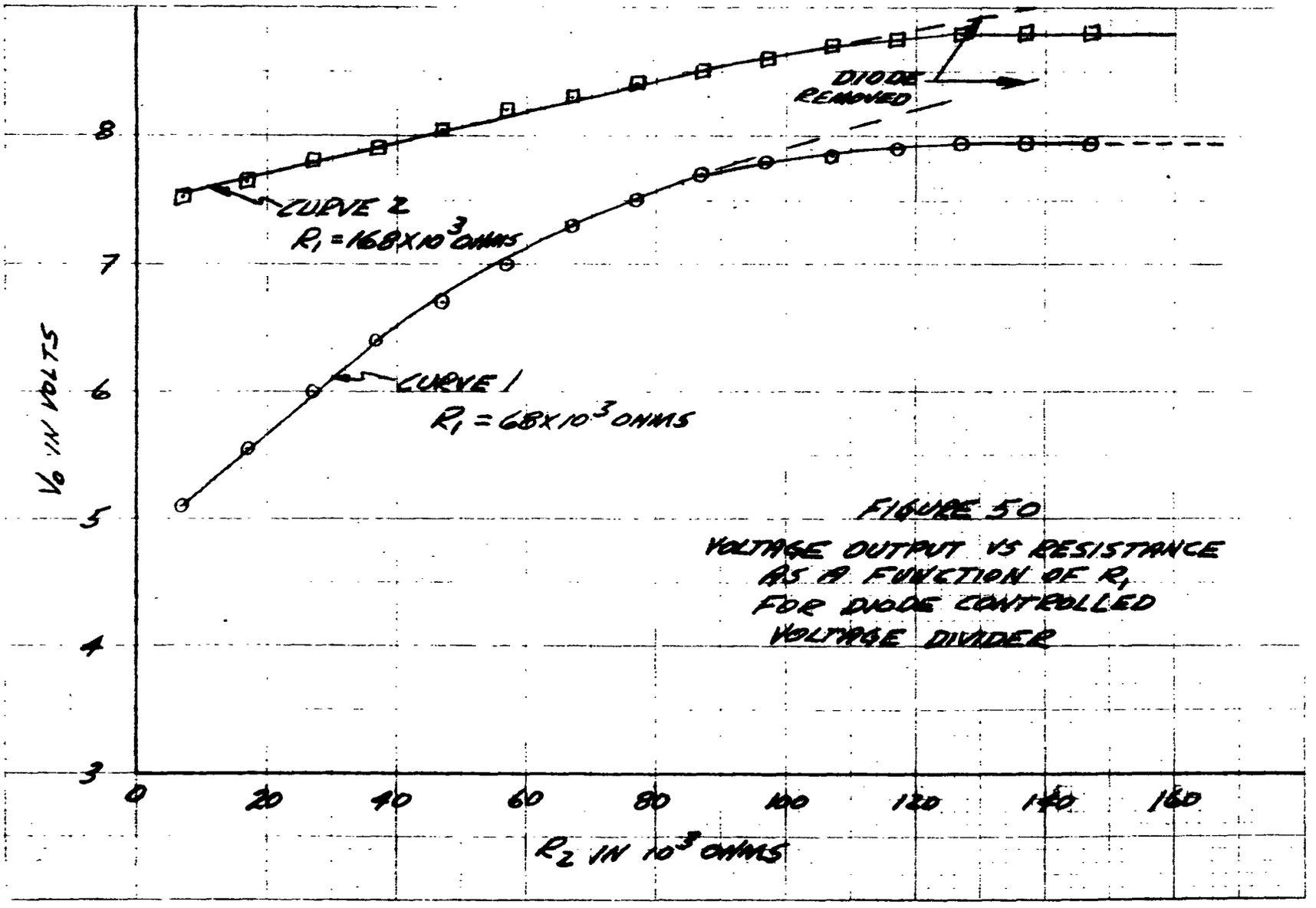
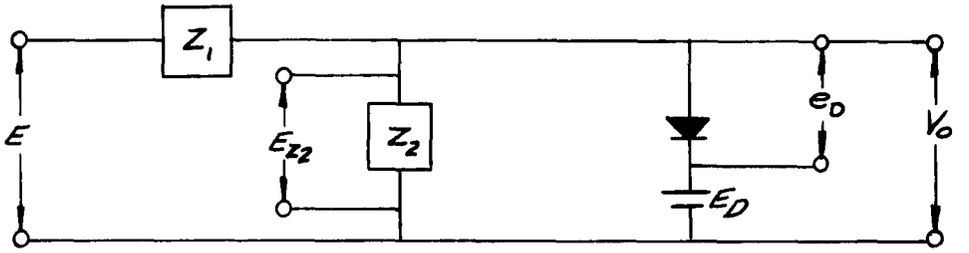


FIGURE 50

VOLTAGE OUTPUT VS RESISTANCE AS A FUNCTION OF R_1 FOR DIODE CONTROLLED VOLTAGE DIVIDER

When E_{Z2} tries to become more positive than E_D, then Diode D_1 conducts, maintaining $E_{Z2} = e_D^+ + E_D$. Under these conditions Z_2 can continue to change with temperature with no change in voltage across it. Figure 50 shows some actual curves of voltage versus R_2, when the diode is in the circuit and is not in the circuit.

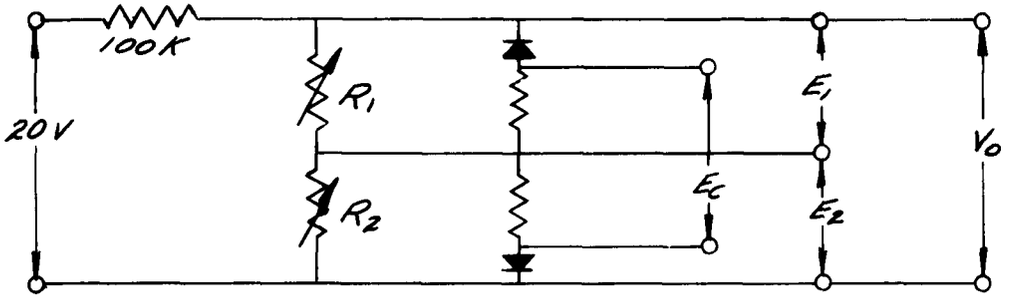
If Diode D_1 is reversed in polarity the circuit shown below is obtained.



DIODE CONTROLLED VOLTAGE DIVIDER
Figure 51

The effect of D_1 in Figure 51 is exactly the opposite of the effect of D_1 in Figure 49. E_{Z2} cannot become less than $E_D + e_D$, but can become greater.

Another method of accomplishing diode voltage control is shown in Figure 52.



DIODE CONTROLLED VOLTAGE DIVIDER
Figure 52

As resistance increases V_o becomes greater if Diodes D_1 and D_2 are not present and as resistance decreases, voltage V_o decreases if D_1 and D_2 are not present.

Figure 53 shows the effect of D_1 and D_2 on the output voltages E_1 and E_2.

Figures 54 and 55 show the effect of varying E_c on the output voltage. Another possible configuration using this same schematic is to place a diode in the Z_1 leg of the circuit as shown in Figure 56.

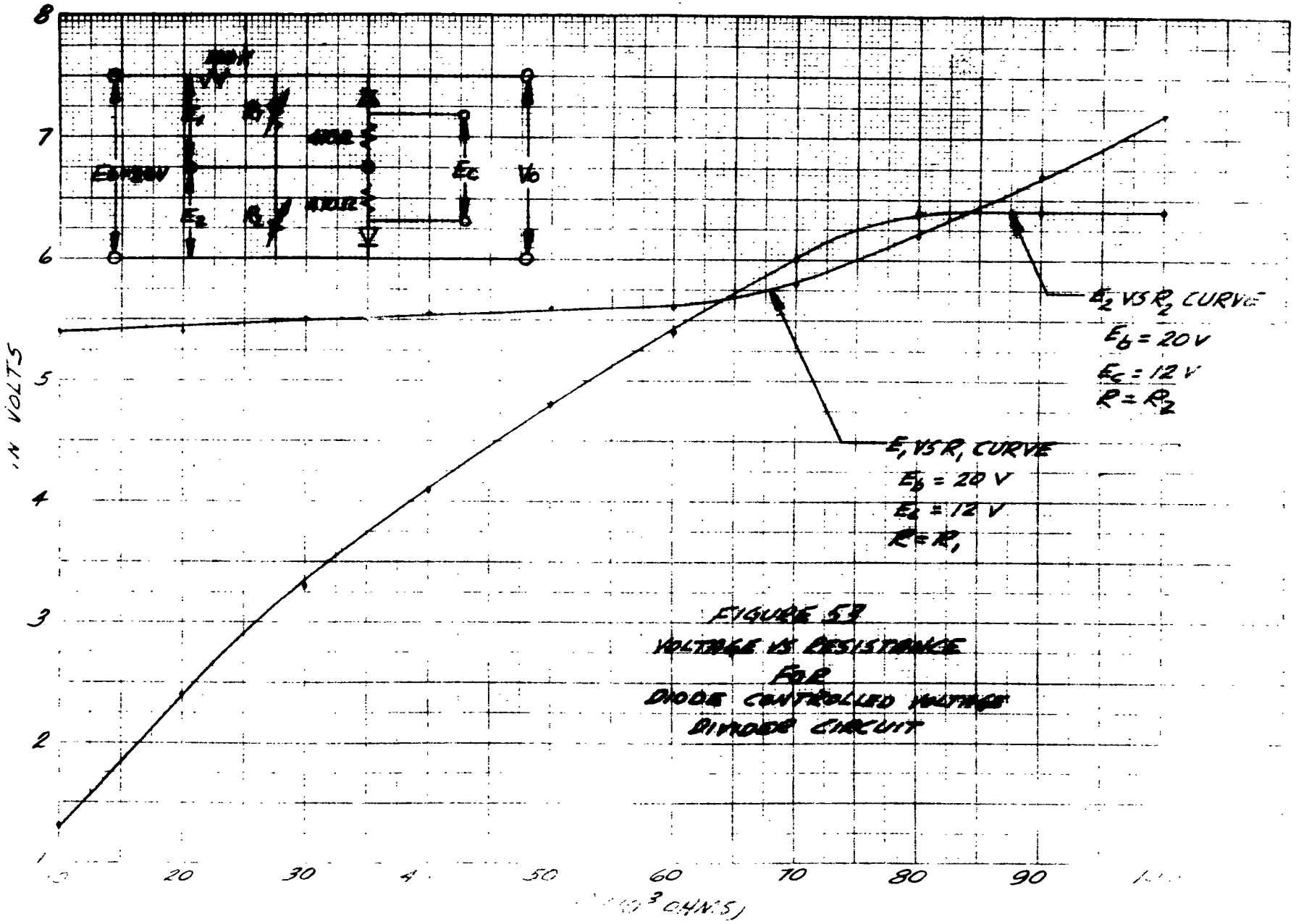


FIGURE 53
VOLTAGE VS RESISTANCE
FOR
DIODE CONTROLLED VOLTAGE
DIVIDER CIRCUIT

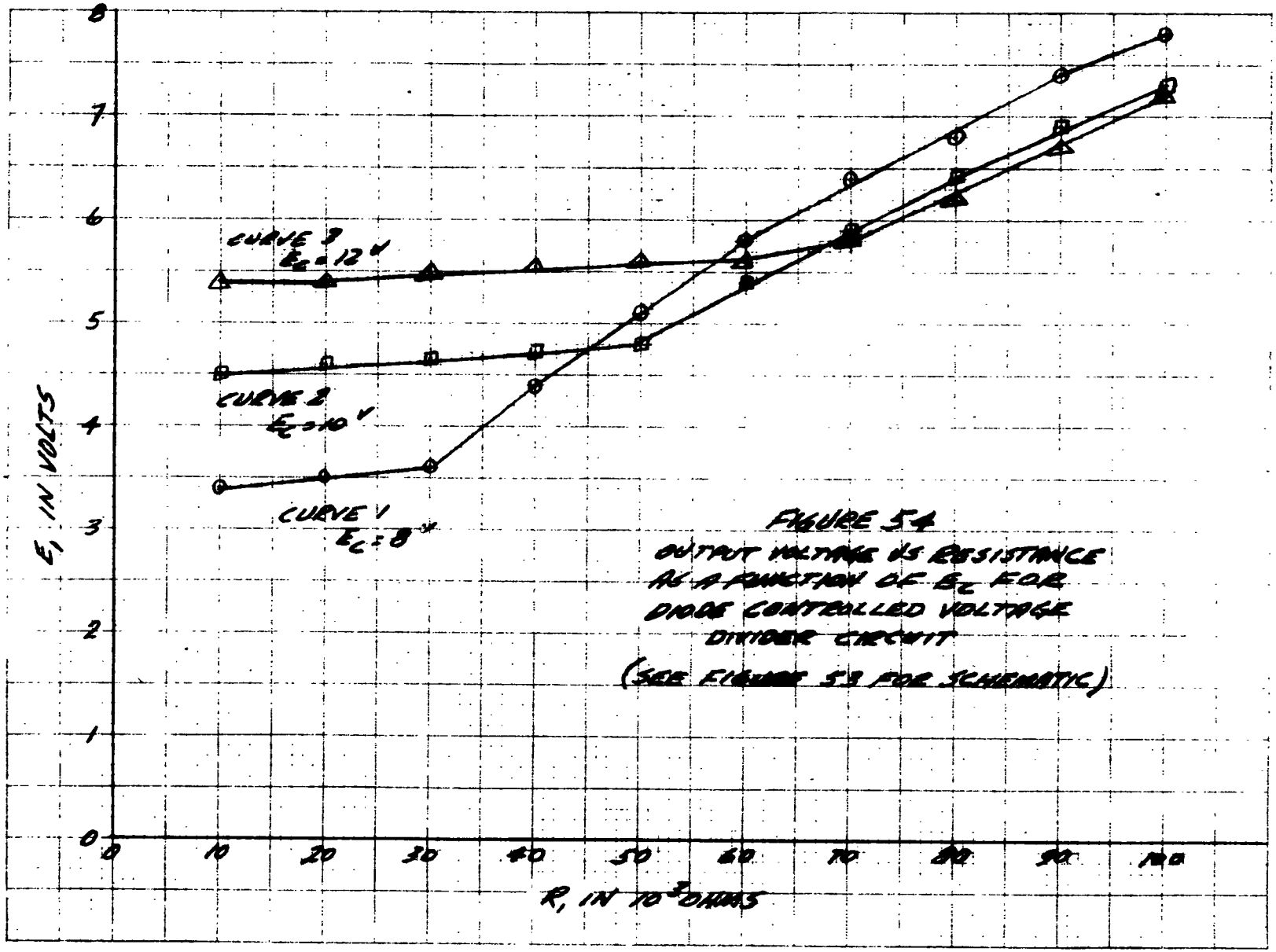


FIGURE 54
OUTPUT VOLTAGE VS RESISTANCE AS A FUNCTION OF E_c FOR DIODE CONTROLLED VOLTAGE DIVIDER CIRCUIT
(SEE FIGURE 53 FOR SCHEMATIC)

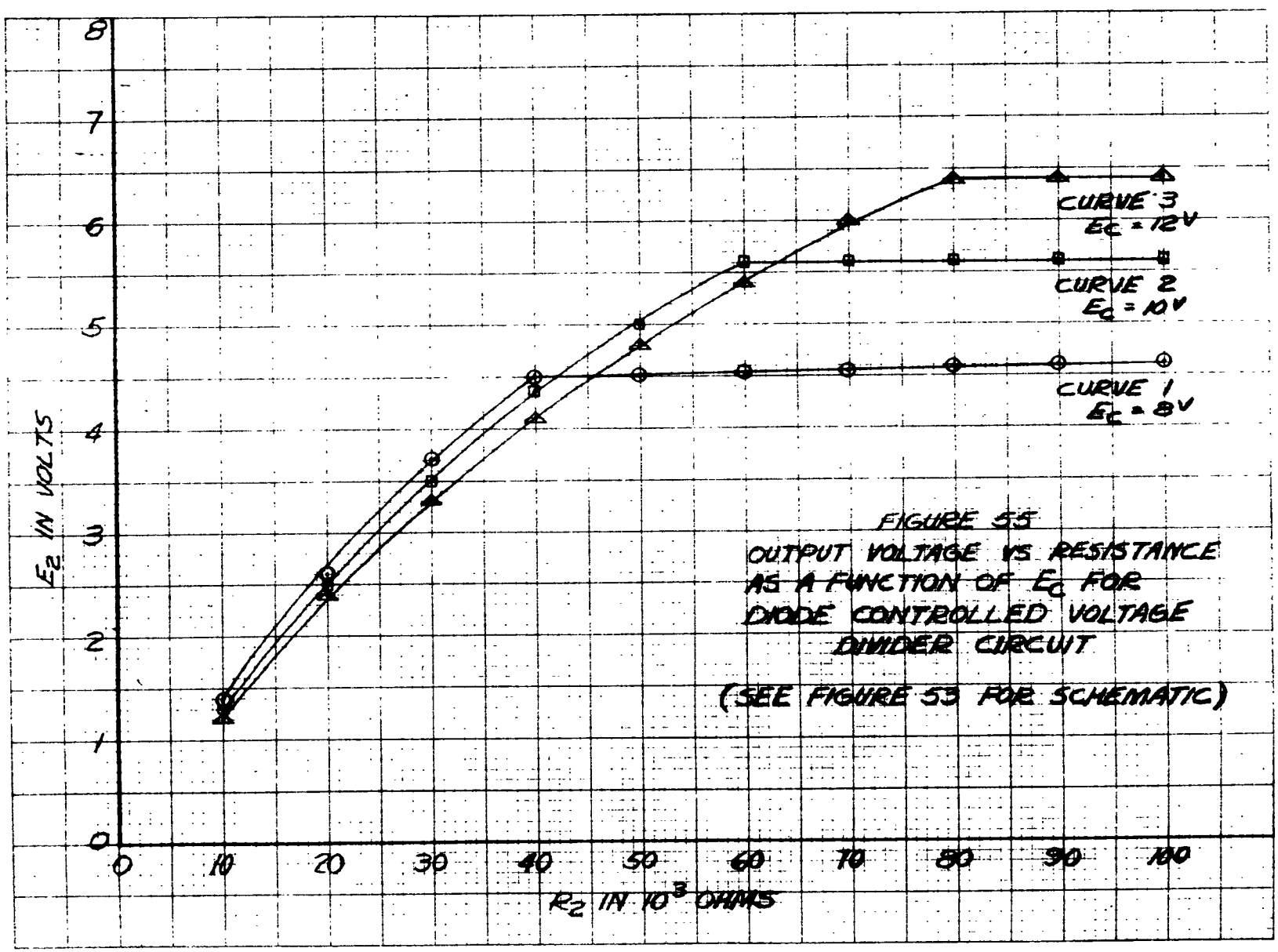
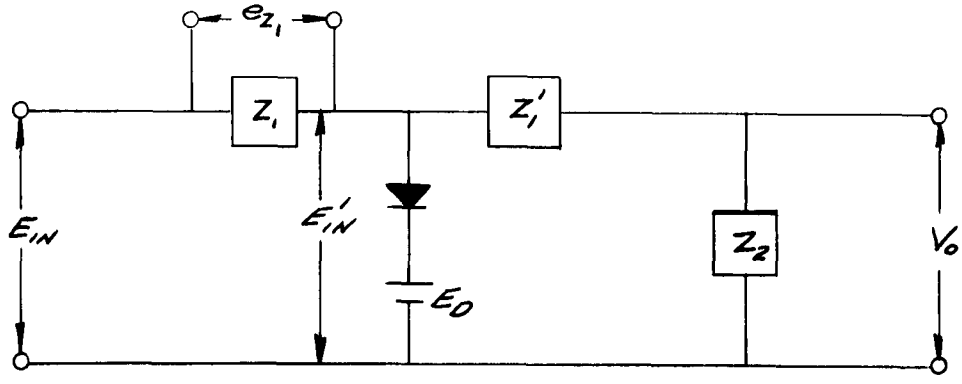


FIGURE 55
OUTPUT VOLTAGE VS RESISTANCE AS A FUNCTION OF E_c FOR DIODE CONTROLLED VOLTAGE DIVIDER CIRCUIT

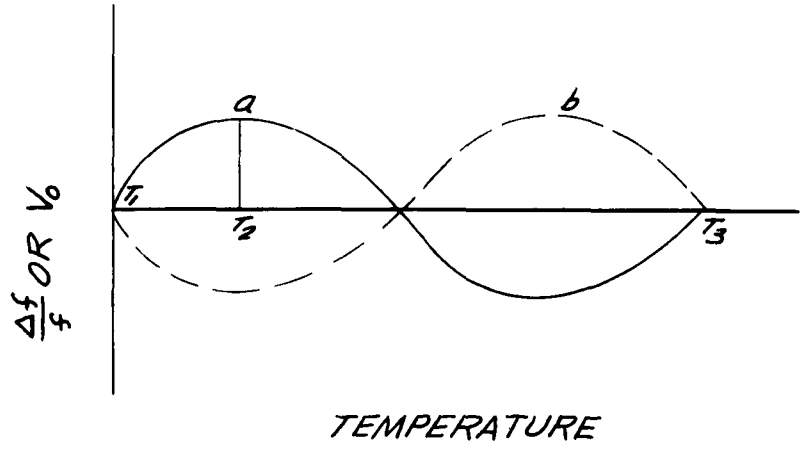
(SEE FIGURE 53 FOR SCHEMATIC)



DIODE CONTROLLED VOLTAGE DIVIDER
Figure 56

By using various combinations of this type of voltage control, many different V_o functions can be generated. The major use of this type of voltage control was intended for the following specific case of TC crystal oscillator.

Assume that compensation of a crystal using the varicap method with a temperature curve as shown in Figure 57a is desired,--where T_1 is the minimum temperature and T_3 is the maximum temperature and T_2 is the lower turning point. If varicap compensation is used, then the required V_o versus temperature curve is similar to the inverted curve of Figure 57a as shown in Figure 57b. A voltage divider is to be used to supply V_o.



COMPENSATION CURVES

Figure 57

To generate a curve such as shown in Figure 57b, Z_1 and Z_2 will basically be as shown in Figure 58b and 58c respectively.

Below T_2 at T_1, R_{t_1} has the most effect but as $T \rightarrow T_2$, R_{t_2} also has some effect. Similarly, at T_3, R_{t_2} is the control element but as $T \rightarrow T_2$, R_{t_1}, also has some effect. Therefore, for some ΔT around T_2 both thermistors have effect. This complicates and in some cases makes it almost impossible to match the required V_o versus T curve.

To eliminate this interaction in the ΔT, the scheme of voltage control using diodes can be employed as in Figure 58d.

At T_1, the equation governing V_o is shown by Equation (1).

$$(1) \quad V_o = (E_{D_1} - e_{D_1}) \left(\frac{R_{T_a} + R_a}{R_{T_a} + R_a + R_1} \right)$$

As the temperature increases and temperature T_2 is reached, D_1 cuts off and D_a is made to conduct. Above T_2 Equation (2) describes the output voltage, V_o.

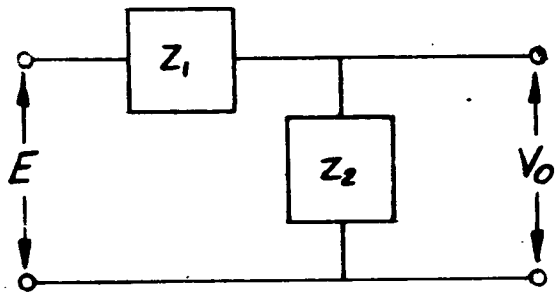
$$(2) \quad V_o = \frac{ER_a}{R_x + R_2 + R_a} + (E_{D_a} - e_{D_a}) \left(1 + \frac{R_a}{R_x + R_2 + R_a} \right)$$

NOTE: $R_x = \dfrac{R_1 R_{T_1}}{R_1 + R_{T_1}}$

As can be seen by inspection of Equations (1) and (2)only one variable exists in each equation if the change in e_D is considered negligible. In Equation (1), E_{t_a} is the only variable and in Equation (2) R_x or R_{T_1} is the only variable. This eliminates the matter of the considering the effects of both transistors over a ΔT.

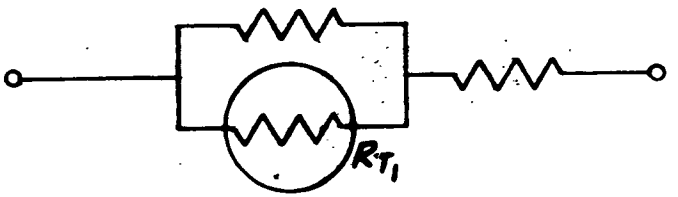
Equation (3) is the equation that describes V_o in the absence of D_1 and D_2.

$$(3) \quad V_o = \frac{E (R_{T_a} + R_a)}{(R_x + R_{T_a} + R_2 + R_a)}$$

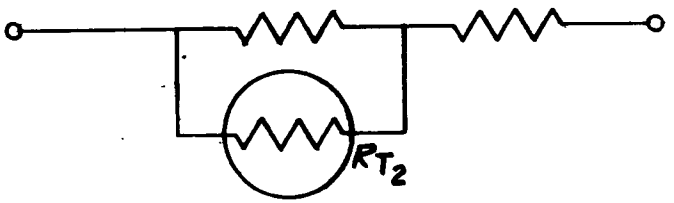


(a)

BASIC VOLTAGE DIVIDER SCHEMATIC

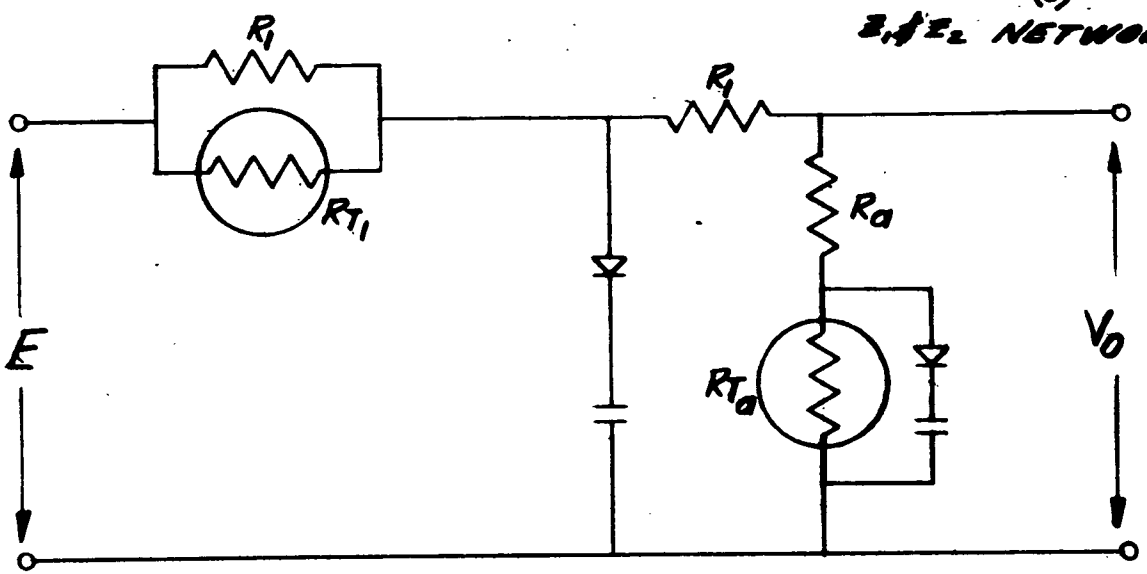


(b) Z_1



(c) Z_2

Z_1 & Z_2 NETWORKS

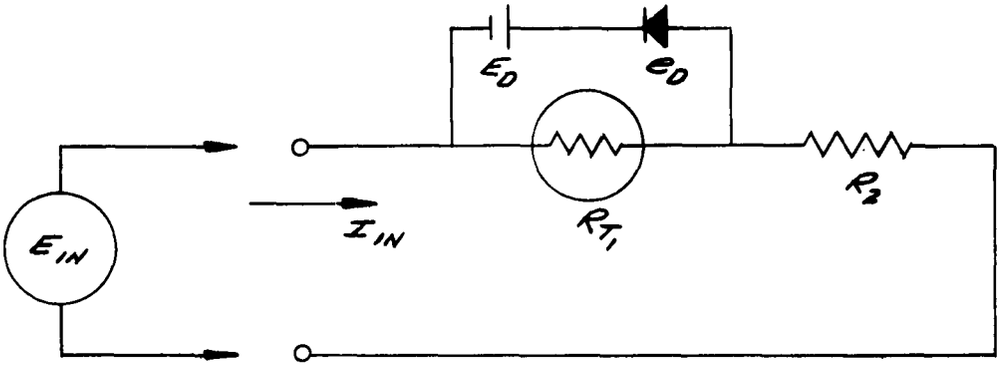


(d) COMPLETE VOLTAGE DIVIDER

DIODE CONTROLLED VOLTAGE DIVIDERS

This method of voltage control can also be used in the diode capacitor method of compensation. Also the transistor method of compensation can utilize this method to eliminate the effect of a thermistor in Z_1 and Z_2 at a given temperature.

The circuit described above can also be considered as a non-linear resistance generator. Assume a circuit as shown in Figure 59.

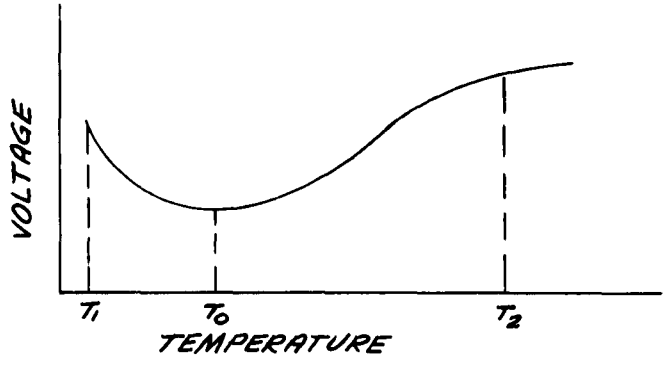


NON-LINEAR RESISTANCE GENERATOR
Figure 59

Diode D_1 has no effect upon the circuit as long as e_D is negative or zero. The equation for R_{in} is in this case $E_{in}/I_{in} = R_{in} = (R_{T_1}+R_2)$. If e_D is positive or zero, the equation for R_{in} becomes the following: $E_{in}/I_{in} = R_2 + (E_E - e_D)/I_{in}$. This term for input resistance no longer contains R_1, and it is therefore effectively out of the circuit when the above conditions are satisfied. This non-linear resistance circuit is useful in the transistor method of compensation.

The second method, Diode Method b, of generating a non-linear voltage function utilizes a zener voltage-regulating diode. Essentially, Method b is the same as is needed. This is due to that fact that a zener diode conducts at a given reverse bias, E, changing its impedance from a very large value to a very low value. Zener diodes can be used to generate almost the same voltage functions as a diode and battery.

Assume a voltage divider as shown in Figure 58a, 58b, 58c, where Z_1 and Z_2 are thermistor-resistor networks. Using NTC thermistors, Z_1 and Z_2, always decrease in magnitude as temperature increases. Also assume that a V_o versus temperature curve must be generated as shown below.

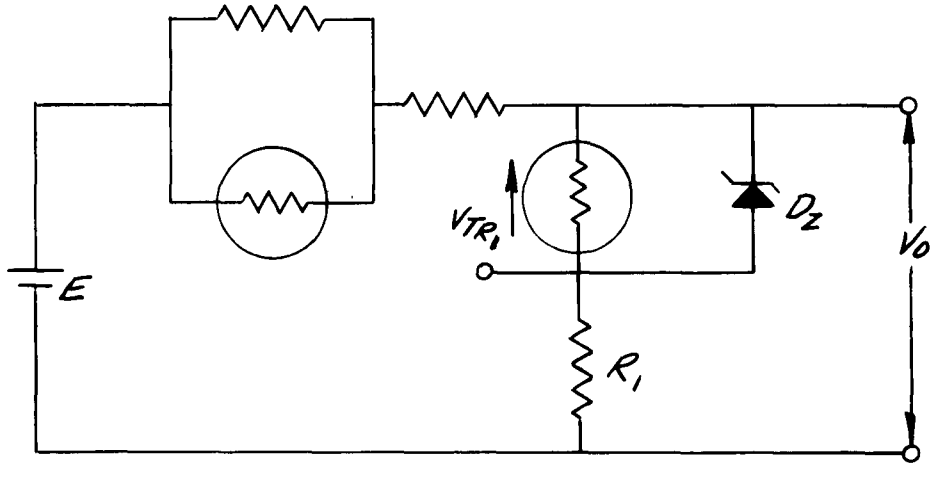


VOLTAGE Vs TEMPERATURE CURVE
Figure 60

At T_1, the change in V_o is almost entirely determined by R_{T_2}, but R_{T_2} and R_{T_1} both have effect at T_2. Therefore, R_{T_1} also determines the change in V_o.

Thus for temperatures around T_o, V_o is dependent on both R_{T_1} and R_{T_2}. By using zener diodes the impedance of V_o on R_{T_1} can be limited to a given temperature range and the dependence of V_o on R_{T_2} can be limited to another temperature range.

Limiting the range of effect of R_{T_2} can be accomplished by the following circuit.

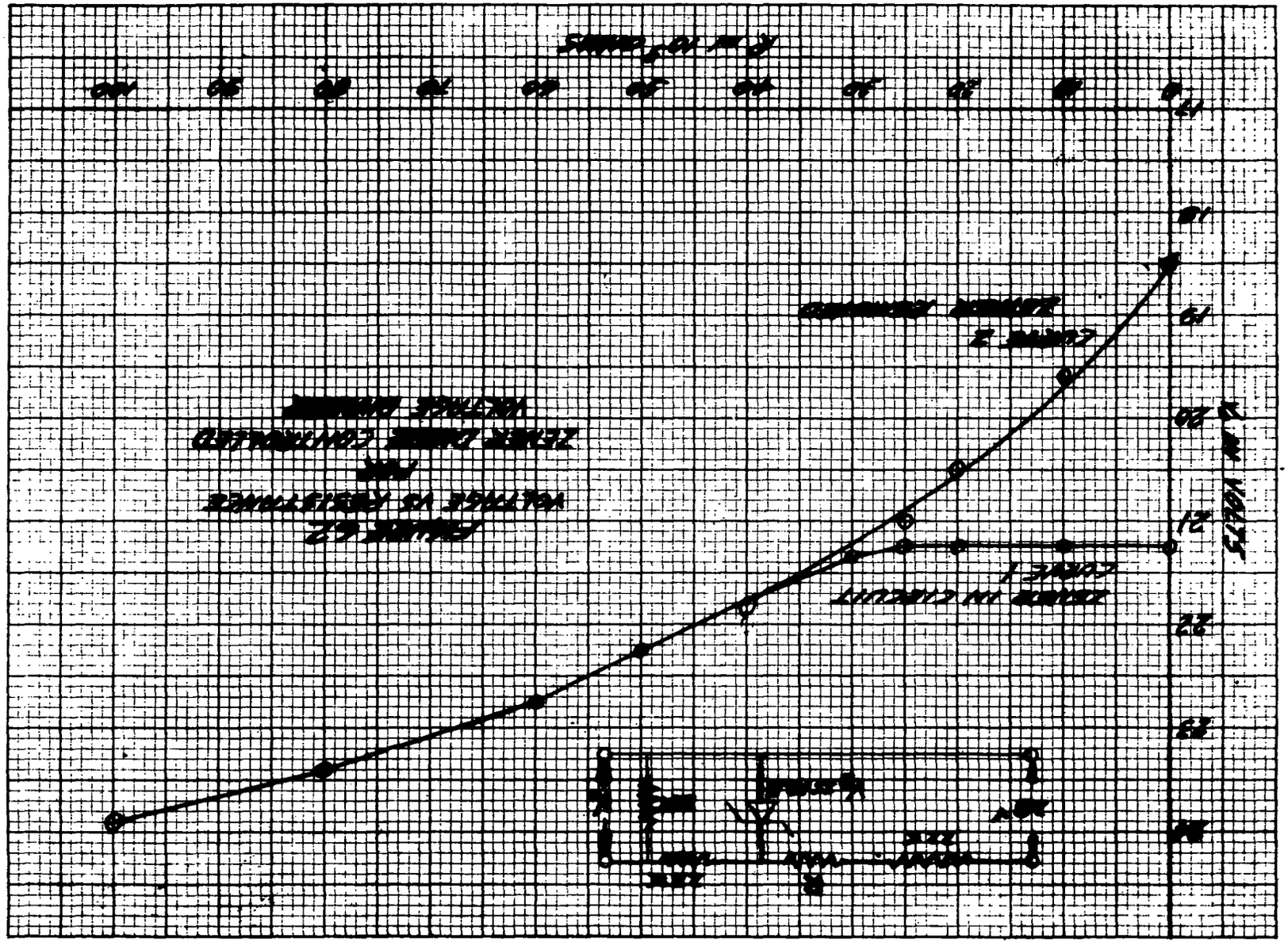


ZENER DIODE CONTROLLED
VOLTAGE DIVIDER
Figure 61

Various methods of using the zener diode to control voltage can be devised. Figures 62, 63, and 64 show the results of generating a non-linear voltage output using zener diodes.

The zener diode method has the advantage that only one voltage source is required, but has certain characteristics that may or may not be disadvantageous. One characteristic that the zener diode is voltage polarity dependent and another is that zener diode has a discrete break-over voltage. If different voltages are required different zener diodes must be used. Also, zener diodes may only be used to limit positive going voltages.

The curves in Figure 65 illustrate the effect of zener diode on a compensated oscillator using the capacitor-diode method of compensation. Curves #1 and #2 in Figure 65 are affected very slightly by the zener diode, but the effect of the dotted curve shows the actual frequency versus temperature characteristics of the oscillator using a supply voltage between 15 and 15.5 volts.



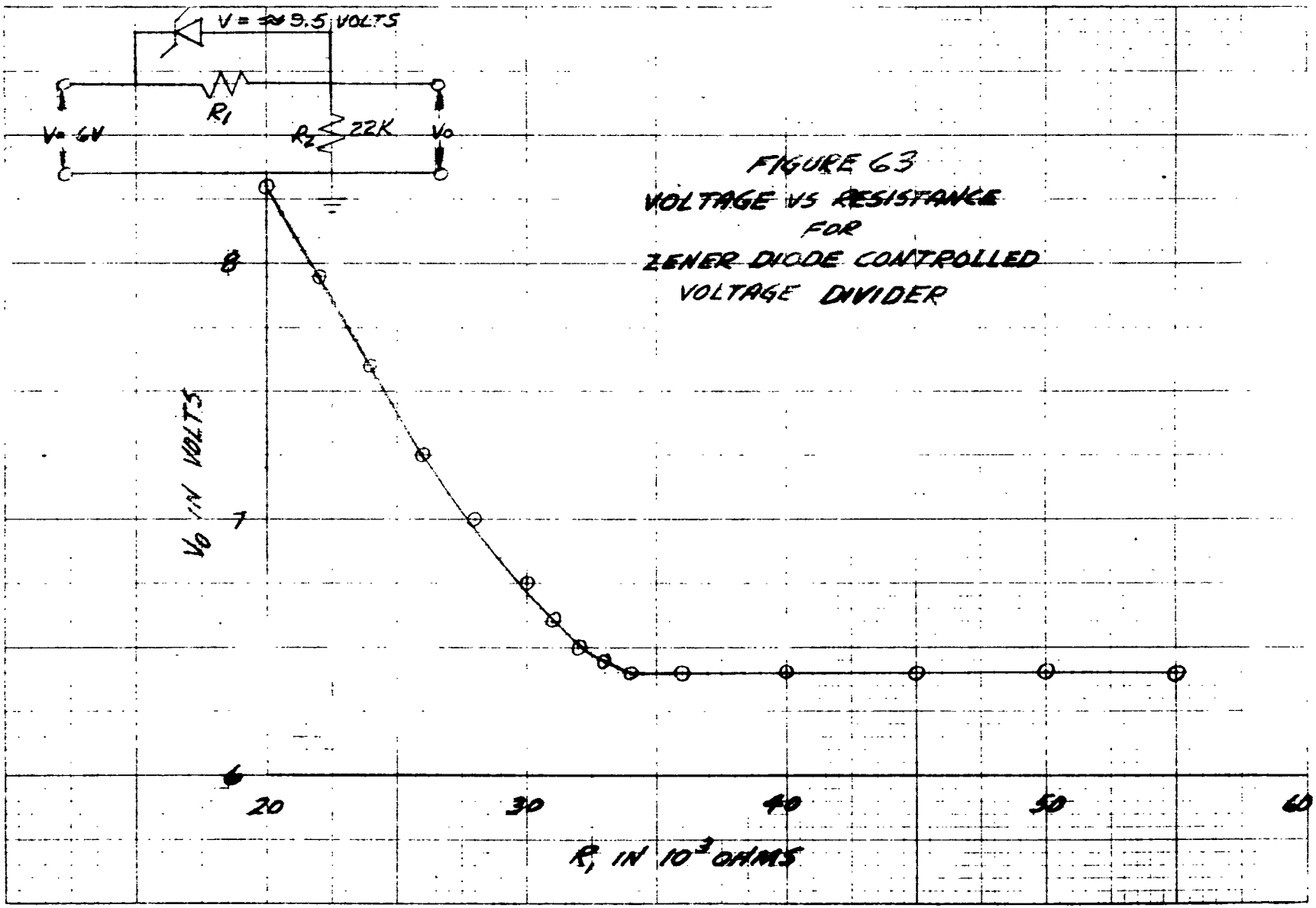
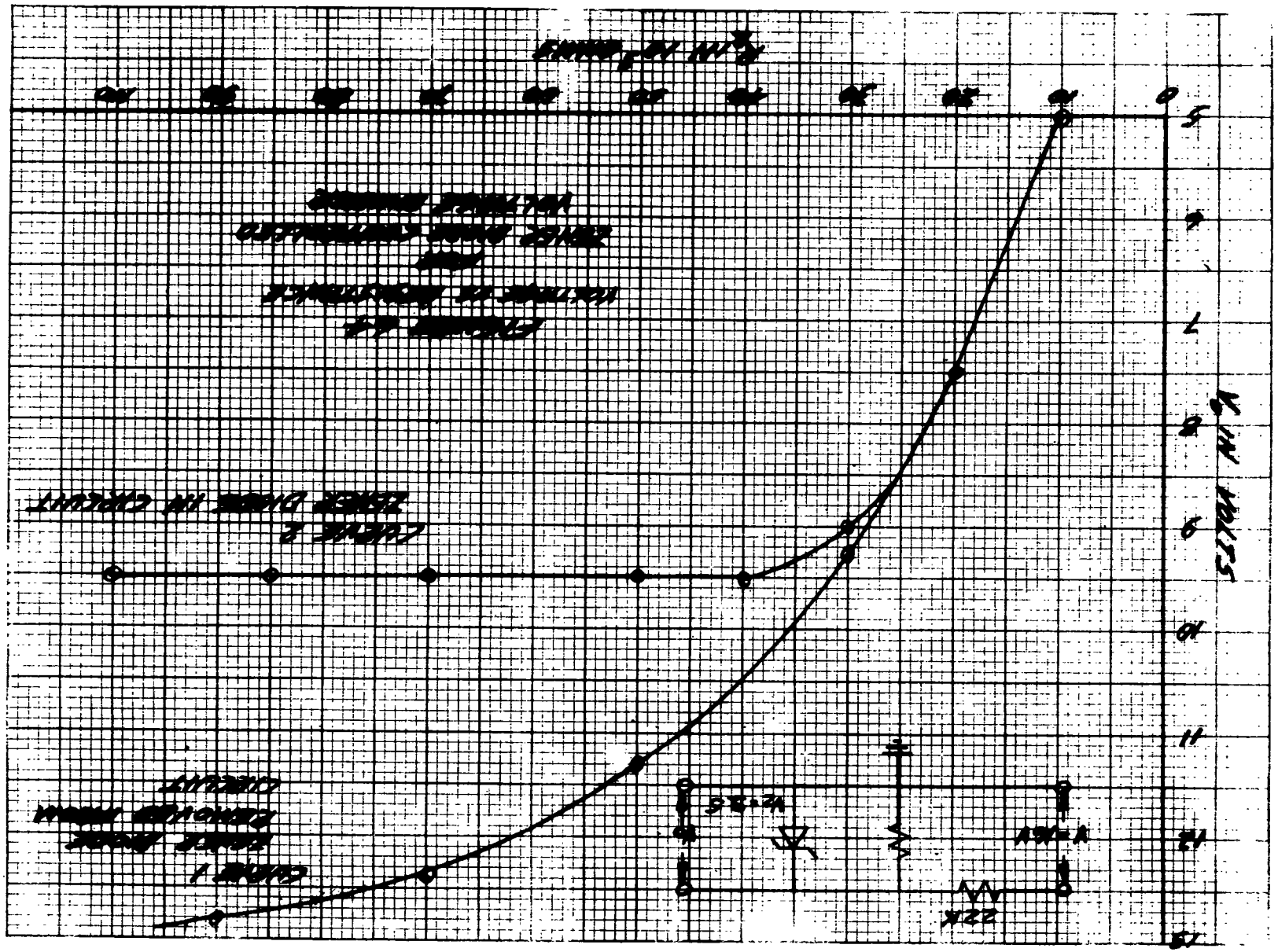


FIGURE 63
VOLTAGE VS RESISTANCE
FOR
ZENER DIODE CONTROLLED
VOLTAGE DIVIDER



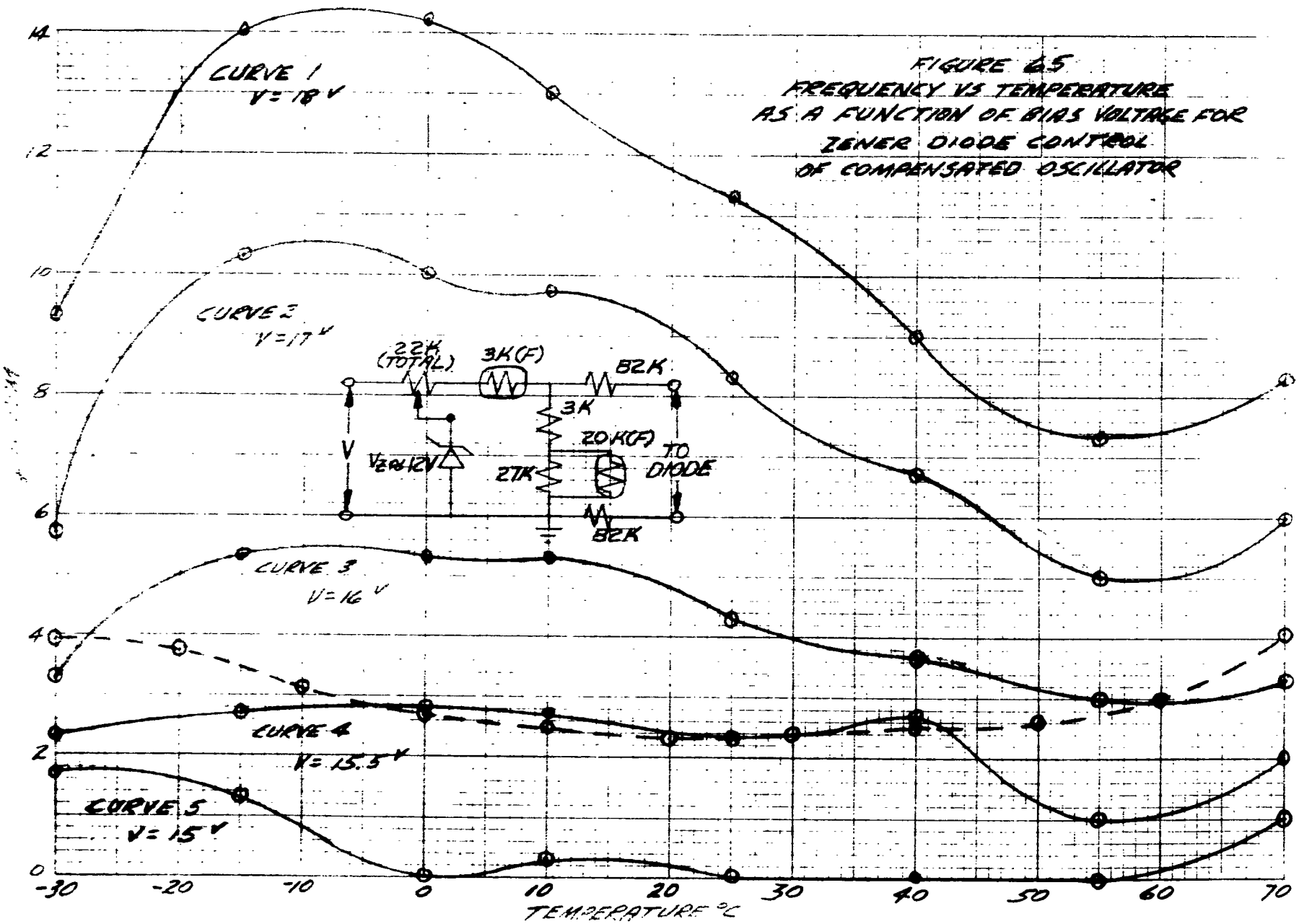


FIGURE 45
FREQUENCY VS TEMPERATURE
AS A FUNCTION OF BIAS VOLTAGE FOR
ZENER DIODE CONTROL
OF COMPENSATED OSCILLATOR
CURVE 1
V = 18 V
CURVE 2
V = 17 V
CURVE 3
V = 16 V
CURVE 4
V = 15.5 V
CURVE 5
V = 15 V
22K (TOTAL)
3K(F)
82K
3K
20K(F)
TO DIODE
V
V_Z@12V
27K
82K
14
12
10
8
6
4
2
0
-30
-20
-10
0
10
20
30
40
50
60
70
TEMPERATURE °C

4.10 Oscillator Aging Tests

In order to determine the aging with time of compensates ocillators, an aging test program has been initiated. As new compensation methods are tried, oscillators incorporating these methods are placed on aging runs. At the present time, five oscillators are being aged. Three of the five use the transistor method of compensation, one uses the varicap method of compensation, and the other oscillator uses the diode-capacitor method.

The first oscillator to be placed on aging runs used the transistor method of compensation. Figure 66 shows the aging curves for two of the oscillators, Oscillators #1 and #3 whose frequency versus temperature curves are shown in Figures 21 and 22. The other two oscillator aging curves , Oscillators #2 and #4 were not plotted because their frequency varied with room temperature to such an extent that the aging characteristics were not apparent. Oscillator #4 has since been taken off of the aging test.

The next oscillator to be put on aging was one using the varicap method of compensation. Its aging characteristics are shown in Figure 66, Curve #3. The frequency vs temperature characteristics are shown in Figure 13.

The most recent oscillator to be included in the aging test was one using the capacitor-diode method of compensation. Its aging characteristics are shown in Figure 66, Curve #4. The frequency versus temperature curve for this oscillator is shown in Figure 47, Curve #4.

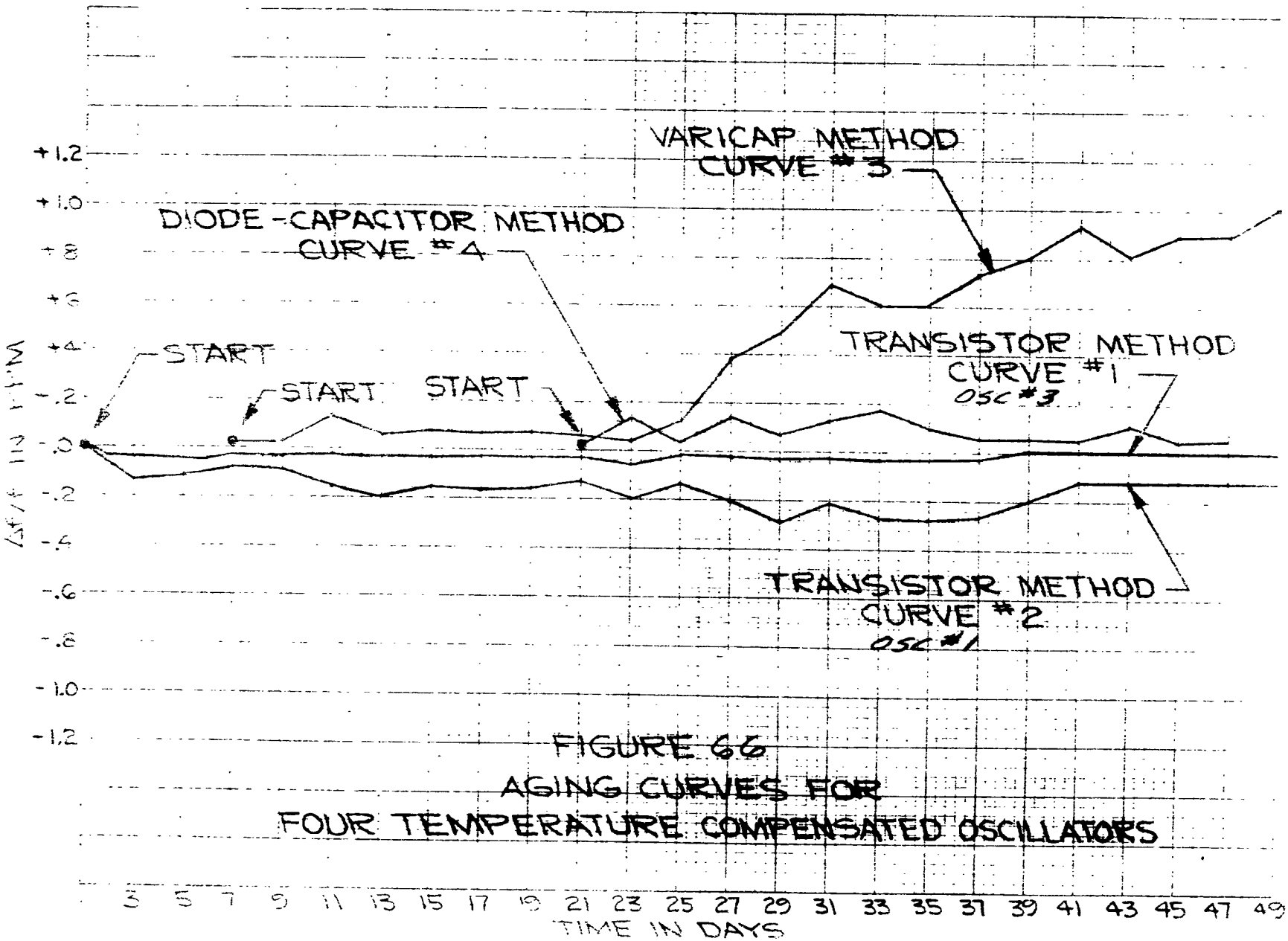


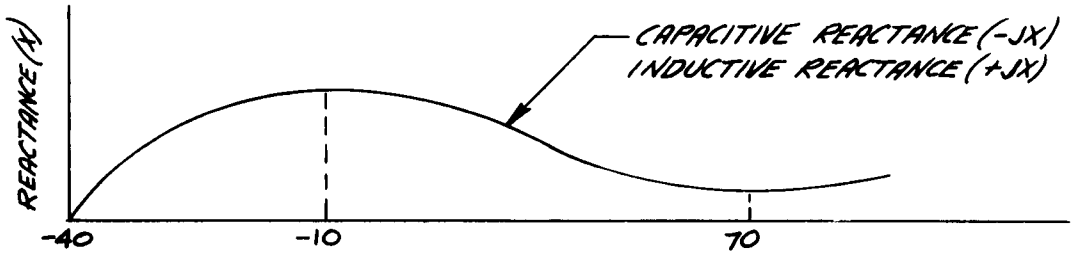
FIGURE 66
AGING CURVES FOR
FOUR TEMPERATURE COMPENSATED OSCILLATORS

4.11 Temperature Sensitive and Special Reactive Components

During the visit made during August by Mr. Layden and Mr. Schodowski the possibility of using temperature sensitive components with characteristics that could be used for compensation was discussed. An investigation has been initiated to determine if such components could be obtained. Figure 67 shows the capacitance and inductive reactance changes required for compensation of a typical AT cut crystal.

TC capacitors with temperature characteristics that change slope can be obtained, but none have been found that are commercially available that are of the right magnitude and turning point. Further inquiries into obtaining special capacitors with the appropriate TC are being made. This will probably involve the necessity of having special dielectric compounds made to obtain the correct TC and capacitance. Coils with the appropriate TC have not been found. Further investigation into the temperature characteristics is being made in an effort to find a suitable material.

An inductor that is not temperature sensitive, but is current controlled is made by the Vari-L Company, Inc. This type of component could be used for temperature compensation of crystal oscillators by providing an appropriate temperature controlled current. The characteristics that this device has does not make it too practical for temperature compensation. The required control current for the variable inductor ranges from 0 to more than 20 ma; there is a hysterisis effect of roughly 5%, and it is relatively large in size and weight. The manufacturer of this device is being contacted to determine the best unit, if any, to use for compensation purposes.



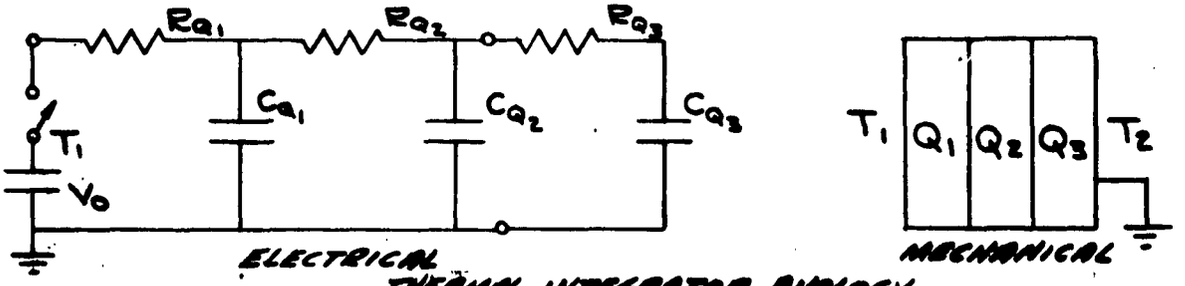
COMPENSATION REACTANCE Vs TEMPERATURE
Figure 67

4.12 Thermal Studies

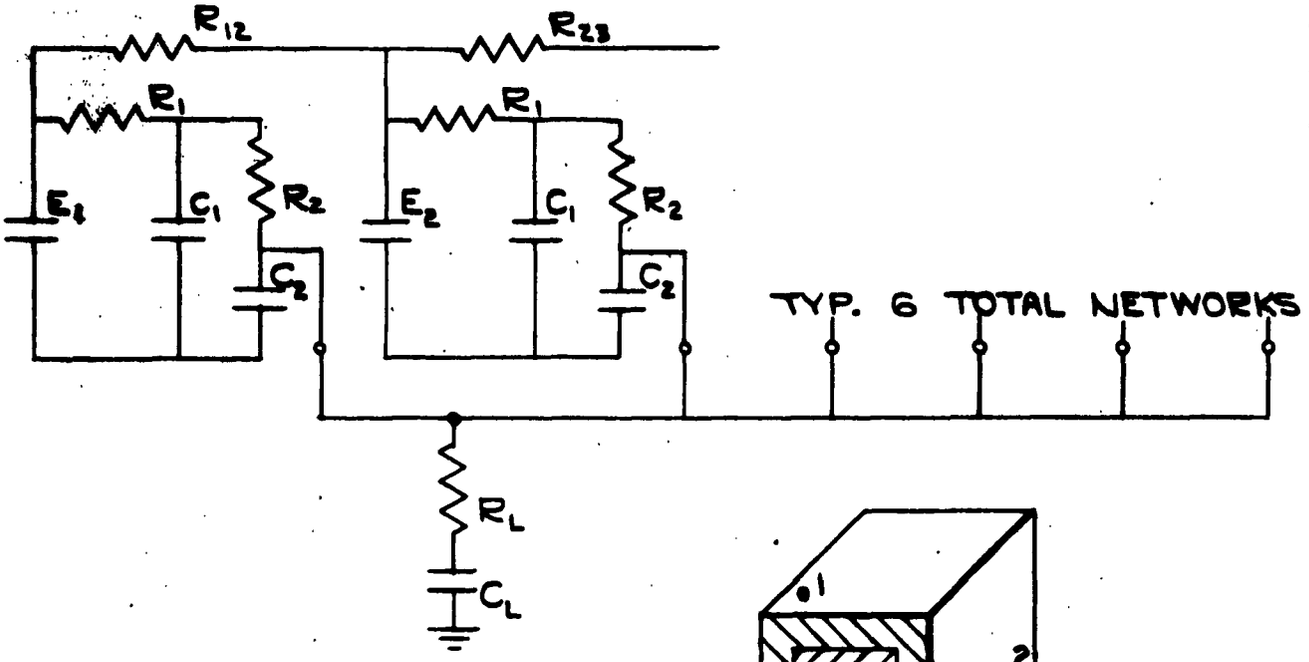
Due to the nature of temperature compensated oscillators, they are subjected to the ambient temperature changes. If the ambient temperature changes rapidly, it is very likely that the crystal and temperature sensitive network will not change temperatures at the same rate due to the difference in the thermal time constant. Where rates of change of temperature are fast enough to cause a temperature difference between the crystal and compensating network, means have to be provided to obtain a thermal delay to the components so that the rate of change seen by the components will never exceed the various component thermal time constants. This in effect requires a thermal integrator. The electrical analog of thermal integrator is shown in Figure 68a. In Figure 68a, assume that $T_1 = T_2$ or that the switch S_1 is open. At some time t_o the switch is closed which is analogus to setting $T_1 > T_2$ by a specified amount. R_1, R_2, and R_3 is the thermal resistance of each material. C_1, C_2, and C_3 represent the thermal stage properties of each material. At some time t_1 after t_o, C_3 is at the same potential as V_o. Conversely at some time t_1 after t_o, T_2 has changed to the value T_1.

Using the analogy presented above, the problem of obtaining an appropriately long thermal time constant for the heat sink becomes electrical rather than mechanical. As can be seen from the simple analogy presented above, the larger R_1 and R_2 are made, the larger the time constant.

Another problem exists in the actual design of a heat sink that was not mentioned previously. In considering a three-dimensional heat sink, the problem of thermal gradients or temperature difference between any two points in space must be considered. Figure 68 (b and c) illustrates the three dimensional electrical and physical analog of a heat sink. Assuming that each of the six surfaces of the heat sink may be at different temperatures, then thermal gradients may also exist at the interior of the heat sink. Therefore, some means must be provided to eliminate the possibility of thermal gradients. This can be accomplished by making material #1 an insulator and material #2 a conductor. The electrical analogy is shown in Figure 68d for one dimension with normalized values of R and C.

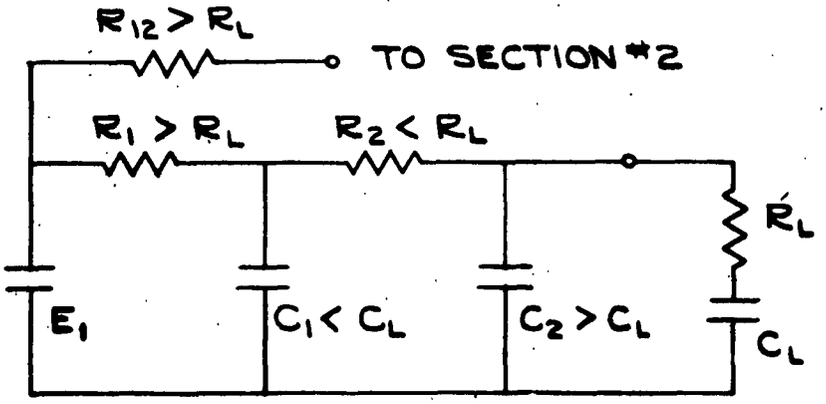


THERMAL INTEGRATOR ANALOGY
(a)



THREE DIMENSIONAL ANALOGY
(b)

(c)



ELECTRICAL ANOLOGY OF ONE SIDE OF HEAT SINK
(d)

HEAT SINK ANALYSIS
FIGURE 68

The R for an insulator will be greater than R_L or the internal component thermal resistance. For a thermal conductor, the R may be quite a bit less than R_L. The C or energy storage of an insulator will be less than C_L and the C of a metal will be greater than C_L. Also the thermal coupling impedance, R_{12}, R_{23}, etc., will be very much greater for an insulator than for a metal.

By using the basic principles presented previously it can be seen that an ideal heat sink would consist of an infinite number of layers of thermal conductors and insulators. In practice, the number of layers will be limited by practical considerations such as weight and volume.

The results of the initial experiments that were made are presented in Figures 69 and 70. At the present time, a mathematical analysis is being considered, such as mounting, weight, volume, method of mounting the crystal and compensation network, and simplicity of fabriaction.

FIGURE 6.9

RESPONSE TO A STEP FUNCTION OF -20 °C TO +50 °C

(a) ALUMINUM BOX ONLY

(b) ALUMINUM BOX AND FIBERBOARD

(c) ALUMINUM BOX, FIBERBOARD AND GLASS WOOL

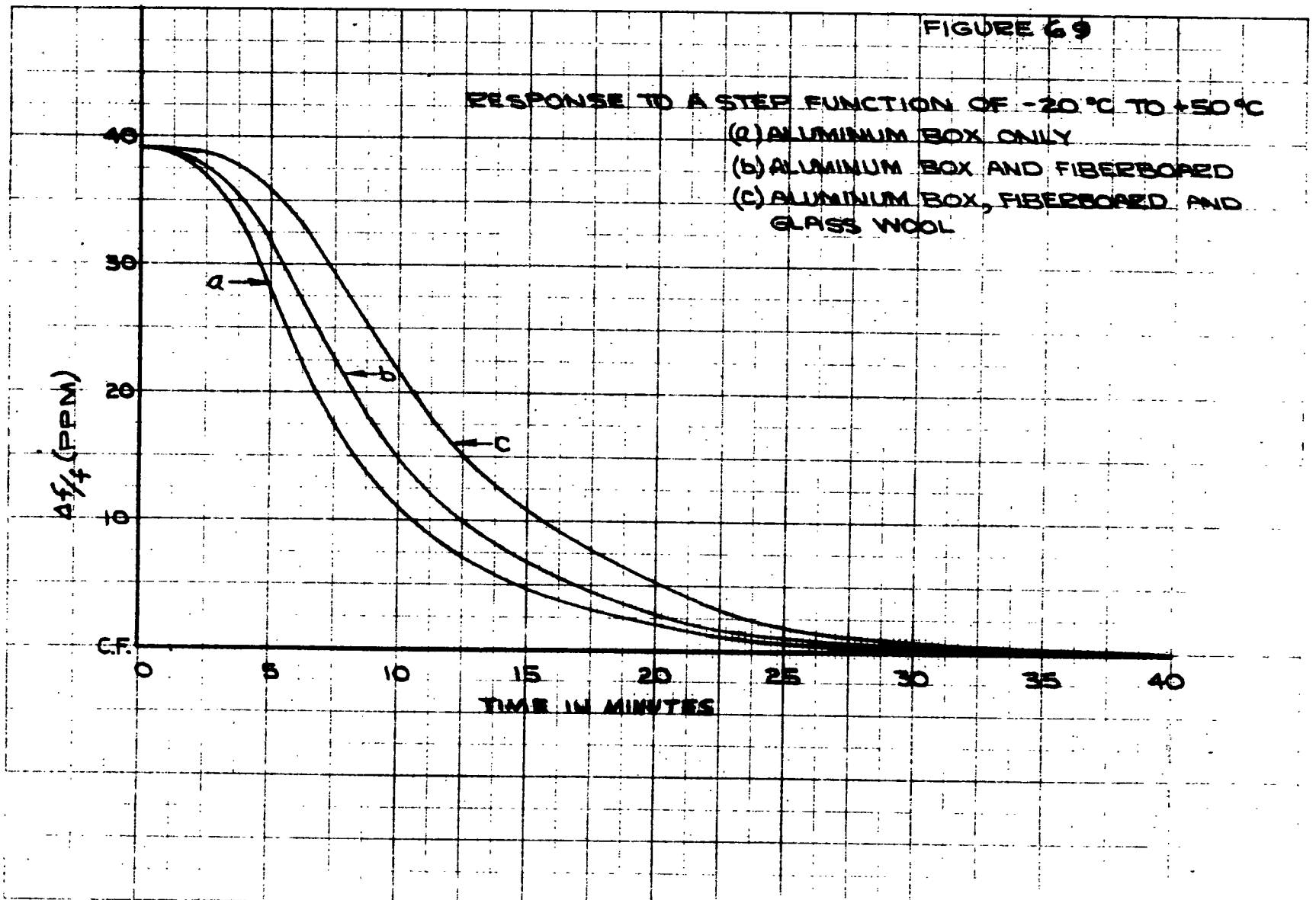
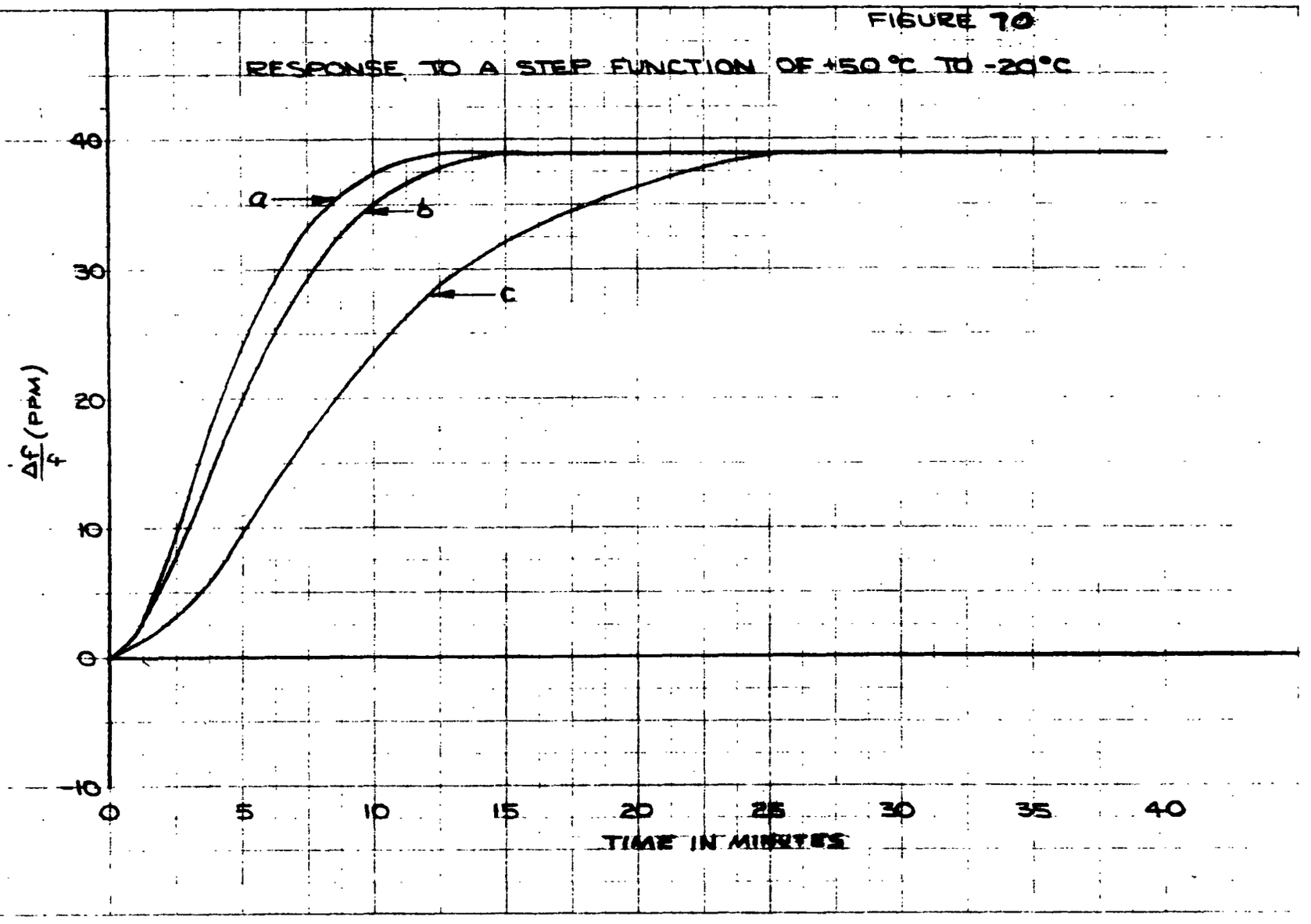


FIGURE 70

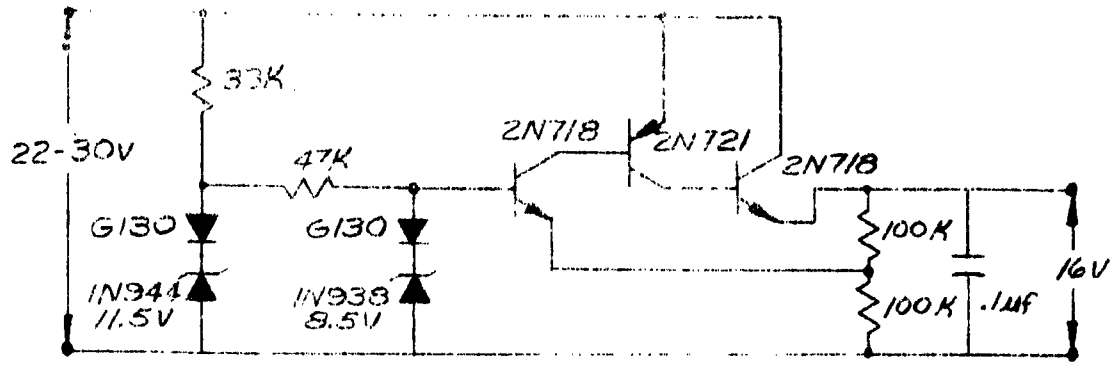
RESPONSE TO A STEP FUNCTION OF +50 °C TO -20 °C



4.13 Voltage Regulators

During the first month of this contract, a short study of voltage regulators was made. The voltage regulation of the B + voltage on an oscillator is very important as can be seen from Figure 26, where the approximate slope of the $\frac{\Delta F}{F}$ versus V curve is 0.7 $\frac{PPM}{volt}$. Therefore, if the B + line voltage is not held nearly constant, an appreciable change in frequency will be observed for a change in the B + voltage. Also, the compensation methods that use voltage dividers are very sensitive to changes in input voltage.

A number of voltage regulators were investigated with varying degrees of success, two of the better voltage regulators that were tried and tested appear in Figure 71. Figures 72 and 73 show the characteristics of the voltage regulator shown in Figure 71b. The regulator in Figure 71a was very similar to the one in Figure 71b, but was not quit as efficient. The variation in output voltage with a variation in input voltage was approximately 10 mv for a change of V_{in} from 22 to 30 volts.


33K
22-30V
47K
2N718
2N721
2N718
G130
G130
100K
16V
IN944
11.5V
IN938
9.5V
100K
.1μf

(A)

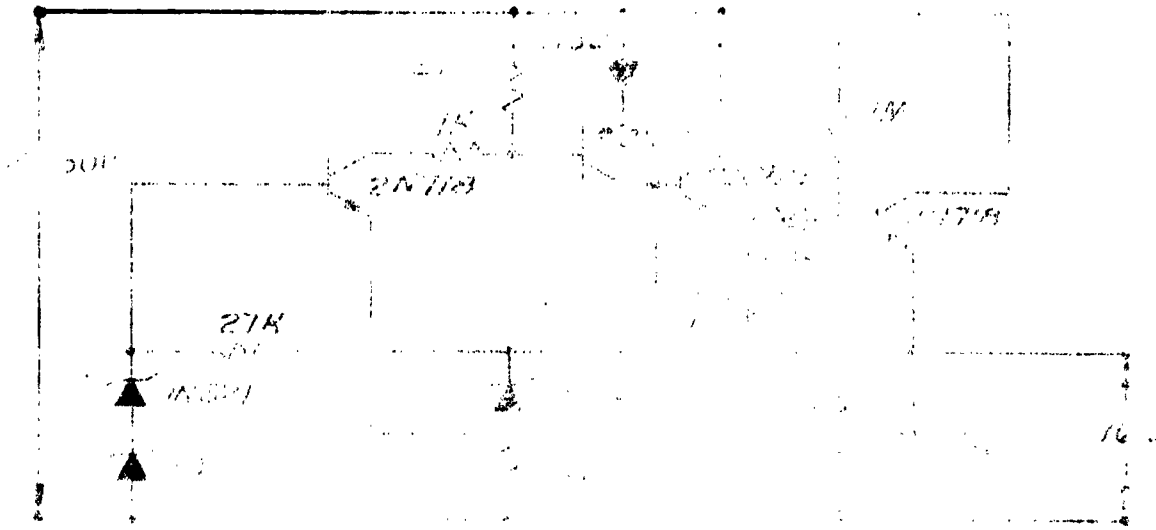
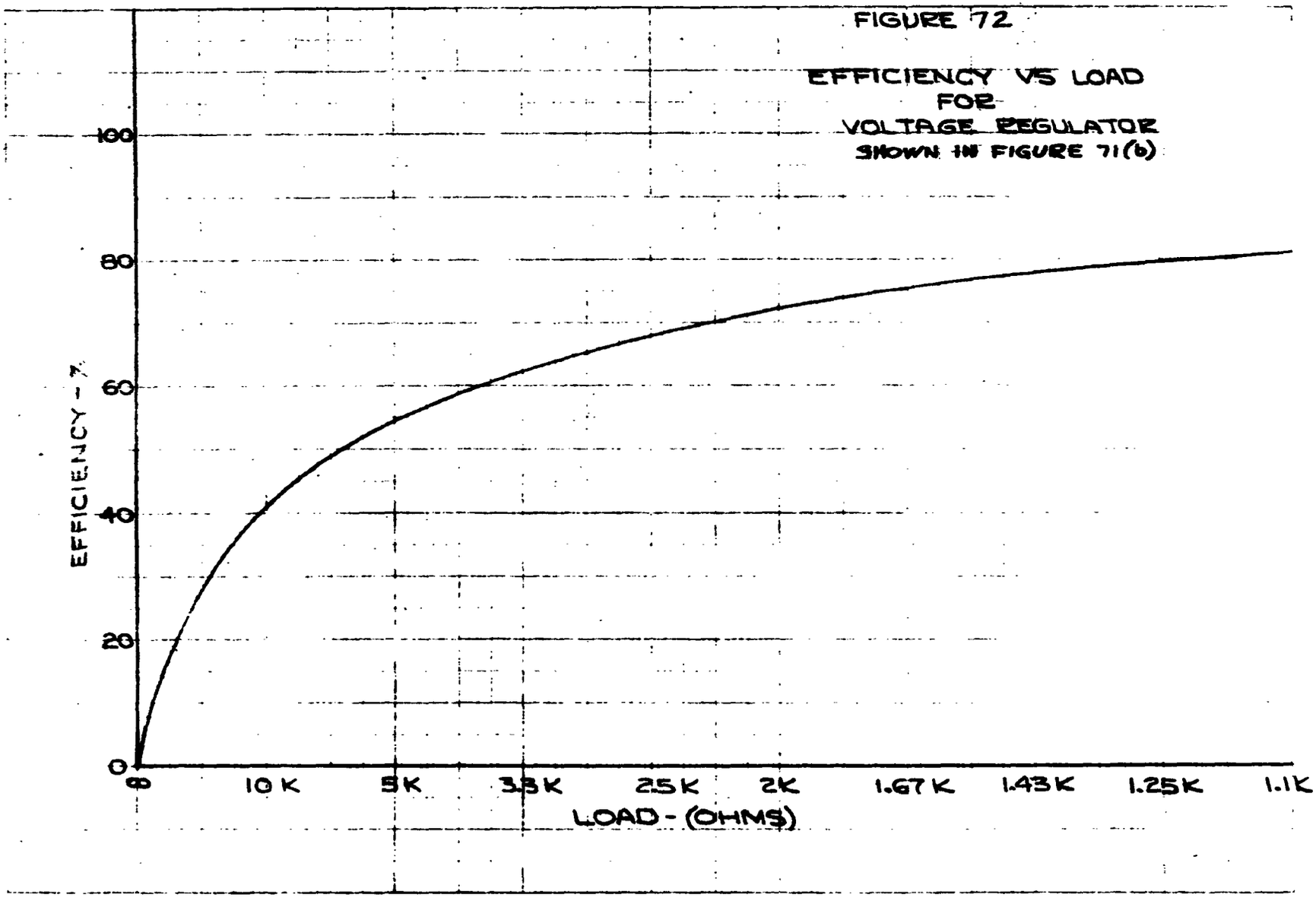

2N718
27K

FIGURE 72

EFFICIENCY VS LOAD
FOR
VOLTAGE REGULATOR
SHOWN IN FIGURE 71(b)



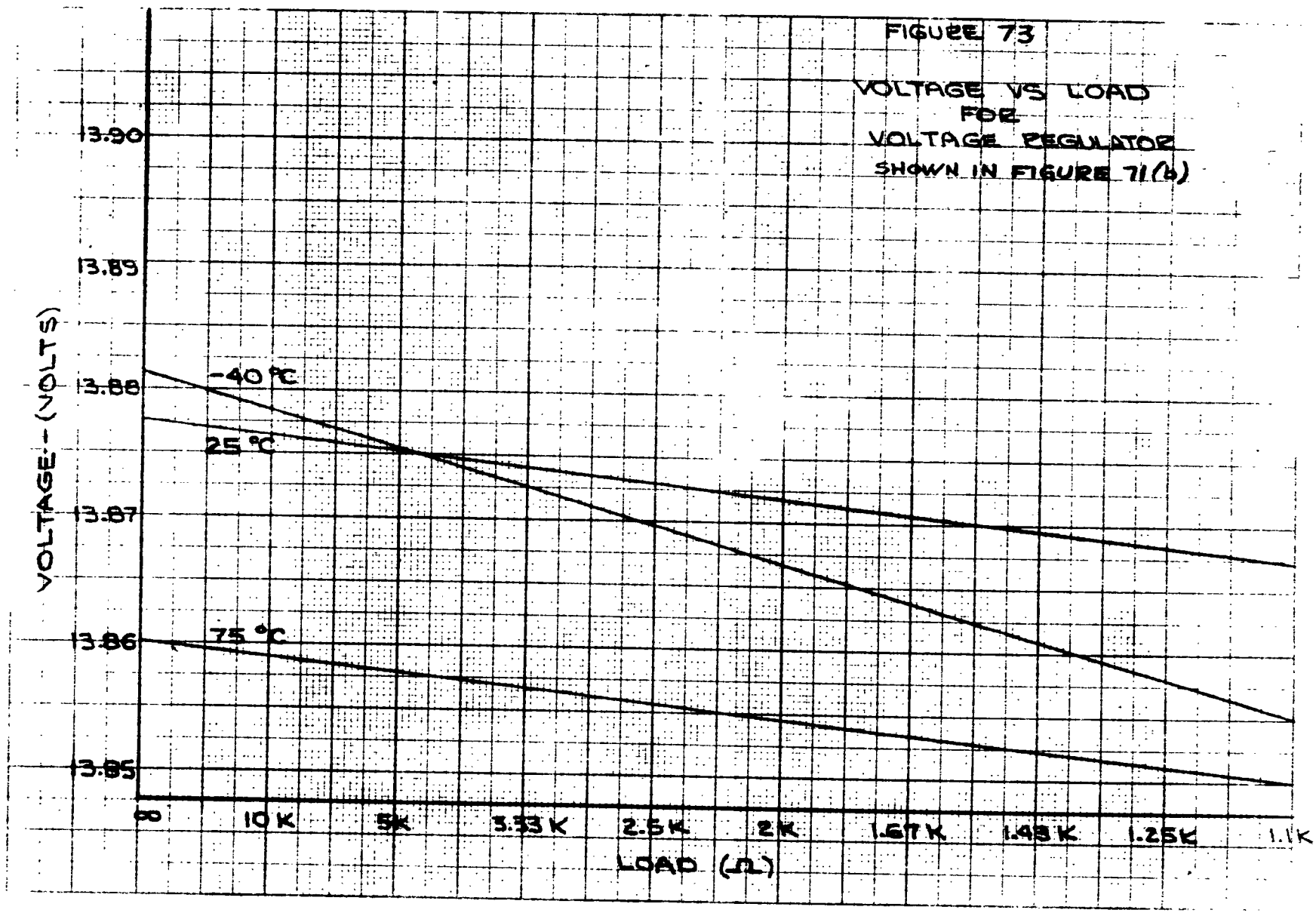


FIGURE 73
VOLTAGE VS LOAD
FOR
VOLTAGE REGULATOR
SHOWN IN FIGURE 71(b)
13.90
13.89
13.88
13.87
13.86
13.85
VOLTAGE - (VOLTS)
-40 °C
25 °C
75 °C
∞
10 K
5K
3.33 K
2.5K
2K
1.67K
1.43 K
1.25K
1.1K
LOAD (Ω)

4.14 Component Data

A survey of the available components that will be used in compensated oscillators has been initiated. The reason for this is that if compensation is to be achieved with a minimum amount of effort, then the component parameters must be known very closely and cannot change under environmental conditions or with time. The following table lists some of the manufacturer's data obtained for various components. The components listed exhibit the best that were found from the data available. Further investigation will proceed as it is determined what components and parameters will be the most critical.

Component	Vendor	Type	Tolerance	Temperature Coefficient	Aging Characteristics
Resistor: Fixed	#1	Wire wound	.05%	± 25 PPM/°C	.27%/1000 hr.
	#2	Wire wound	.25%	25 PPM/°C typical	.1%/1000 hr.
Variable	#1	Wire wound	---	70 PPM/°C	---------
	#2	Wire Wound	---	60 PPM/°C	---------
Capacitor: Fixed	#1	Ceramic	± 10%	10% to 680 pf 15% over 680 pf	---------
	#2	Porcelain	± 1%	25 PPM/°C	.05% drift
	#3	Silver mica	± 1%	100 PPM/°C typical	2% maximum
Thermistor:	#1	---	± 1%	*2.35% to 3.6%	---------
	#2	---	± 1%	*1.4% to 4%	1%/year
	#3	---	± 1%	*1/2% to 5%	.1% to .25%/year
	#4	---	± 2% to ± 10%	*2.5% to 5%	---------

*tolerance on beta

5.1 Conclusions

Progress has been made in determining the characteristics of the different type of compensation techniques. The results so far indicate that additional temperature compensation techniques of quartz crystal oscillators can be devised.

At this time, it is difficult to say which method of compensation will yield the best results. The mathematical analysis of the various types of compensation indicates that all methods can be used to temperature compensate an oscillator. The best compensation obtained has been with the capacitor diode method over the temperature range of 0°C to +60°C.

The effects of component aging have not been investigated sufficiently to arrive at a conclusion as to the total effect that any component parameter change will have on a given compensation technique.

Aging data on compensated oscillators has not been obtained on a sufficient number or for a sufficient length of time to draw definite conclusions. From the data obtained thus far, it appears that the transistor and capacitor diode method of compensation have very little aging effects. The varicap compensated oscillator has aged considerably more than the other two types, but the reason for this is not known as yet.

6.1 Personnel Associated with the Project

The following Engineering personnel have engaged in various activities in conjunction with the project during the report period.

PROJECT DIRECTOR: Dr. Darrell E. Newell, Ph.D — Approximate hours: 110

EDUCATION:

BSEE, Iowa State University, 1952
MSEE, State University of Iowa, 1956
Ph.D. in EE, State University of Iowa, 1958

EXPERIENCE:

June 1961 to present
Dr. Newell is the Senior Engineer in charge of research, design and development of products within the Advanced Electronics Group. Representative projects include; development of new techniques in cryogenic liquid level measurement and flow measurement for missile and space applications, preliminary development of complete propellant management system for Saturn II vehicle, development of new techniques for temperature compensation of crystal oscillators, development of a new crystal type cryogenic thermometer and other internal sponsored development projects directed towards advance applications in space and missile technology.

June 1959 to May 1961
Associate Professor in the Research Section of the Electrical Engineering Department at the State University of Iowa. Some of the projects under his jurisdiction included:

1. Study of temperature compensation circuitry for quartz crystal oscillators.
2. Investigation of the short-term instability of regenerated dividers.
3. Investigation of mechanical refrigerator suitable for cooling quartz crystals.
4. Investigation of Parametric Amplification, Oscillation, Miltiplication and Conversion.
5. Nuclear Gryoscope Project.

1952 to 1959
Dr. Newell was employed by Collins Radio Company, Cedar Rapids, Iowa. During this period when academic endeavors were pressing he was employed as a consultant and the remaining time as a Research Engineer in charge of such projects as propagation, excitation and function generator control problems.

1949 to 1952
Transmission Engineer for WOI-AM-FM-TV

PROFESSIONAL AFFILIATIONS:

1. Member and Officer of Institute of Radio Engineers
2. Registered Professional Engineer of Iowa
3. Member of Iowa Academy of Science
4. Maintains First Class Radio - Television Commercial License

PATENTS:

1. Switching Circuitry
2. Automatic Frequency Control
3. Frequency Stabilizing Networks

PUBLICATIONS:

1. "Research Modulation" published by Collins Radio Company
2. "An Investigation of Noise and Function Generators" published by Collins Radio Company

PROJECT ENGINEER: Richard H. Bangert Approximate hours: 445

EDUCATION:

AA, Keokuk Community College, 1958
BSEE, State University of Iowa, 1961
Graduate work towards MSEE, State University of Iowa

EXPERIENCE:

August 1961 to present
Mr. Bangert is the Project Engineer in charge of the Frequency Synthesis and Control Group. Projects under his direct supervision include:

1. Phase-locked Frequency Dividers
2. Temperature Compensated Oscillators
3. Miniature Oscillators
4. Frequency Standards
5. 50 Mega-cycle Phase-locked Loop System
6. Ultra-stable Telemetering Oscillators
7. Research Study for Signal Corps Temperature Compensated Quartz Crystal Oscillator

February 1960 to August 1961
Mr. Bangert worked as a graduate assistant in the Electrical Engineering Department at the State University of Iowa. Projects included; temperature compensation of quartz crystal oscillator, circuitry design for temperature compensation of quartz crystal oscillators, designed computer program for IBM 7070 to find a means of synthesizing temperature compensation networks.

PROFESSIONAL AFFILIATIONS:

Member of Institute of Radio Engineers

PATENTS:

3 pending-Temperature Compensation of Quartz Crystal Oscillators

TECHNICIANS - Approximate hours: 580

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This contract is supervised by the Solid State and Frequency Control Division, Electronic Components Department, USAERDL, Fort Monmouth, New Jersey. For further technical information, contact the Project Engineer, Mr. Stanley S. Schodowski, Telephone 535-2602 (New Jersey Area Code 201).

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THE BENDIX CORPORATION
PIONEER CENTRAL DIVISION
Davenport, Iowa

FREQUENCY TEMPERATURE COMPENSATION TECHNIQUES
FOR QUARTZ CRYSTAL OSCILLATORS
by R. H. Baugert

Report No. 1, First Quarterly Report, 1 July to 30 September, 1962. 111 pages including figures. Contract No. DA36-039 SC-90782. Unclassified Report.

The approaches of circuit techniques for temperature compensation of oscillators which eliminate the need for precisely controlling the oscillator temperature environment is discussed.

Methods of frequency temperature compensation of quartz crystal oscillators are considered both empirically and analytically. Five different approaches are analysed. The first method utilizes the change in capacitance of a back-biased diode with voltage, the second and third utilizes the change in capacitance of the collector-base junction of a transistor as the bias point changes, the fourth utilizes a "binistor" where the third junction is used as a back-biased diode, the fifth method uses the reactance changes exhibited by a forward-biased diode in parallel with a capacitor.

The results of compensating several oscillators using the above methods are shown. Each method results in frequency-temperature compensation to various degrees of accuracy. Results are also shown on aging tests conducted on the compensated crystal oscillators.

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1. Compensation
   Varicap
   Transistor
   Isolation Stage
   Binistor
   Capacitor-Diode
2. Crystal
3. Oscillators
4. Temperature
5. Stability
6. Aging
7. Voltage

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THE BENDIX CORPORATION
PIONEER CENTRAL DIVISION
Davenport, Iowa

FREQUENCY TEMPERATURE COMPENSATION TECHNIQUES
FOR QUARTZ CRYSTAL OSCILLATORS
by R. H. Baugert

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